Peering into Moore's Crystal Ball:
Transistor Scaling beyond the 15nm node

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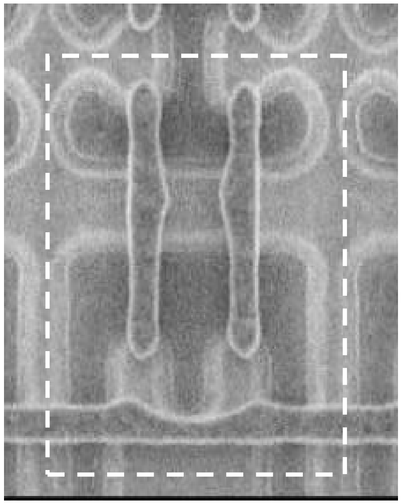
Portland Technology Development
Intel Corporation

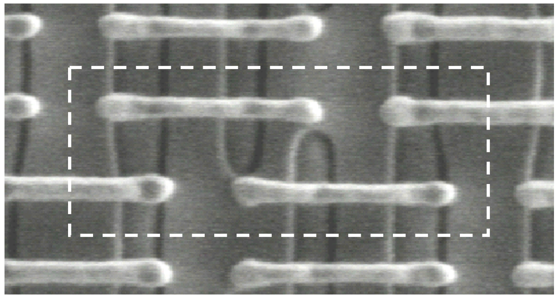
AGENDA

- Scaling
- Gate control
- Mobility
- Resistance
- Capacitance
- Summary

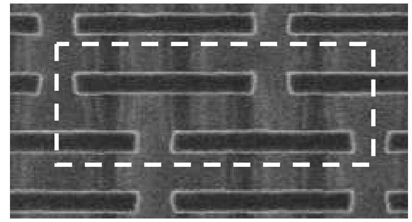
Consistent 2-year scaling



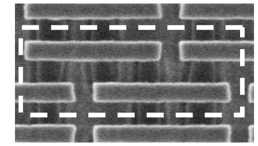
90nm – TALL
1.0 μm^2



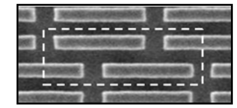
65nm – WIDE - 0.57 μm^2



45nm – WIDE
0.346 μm^2



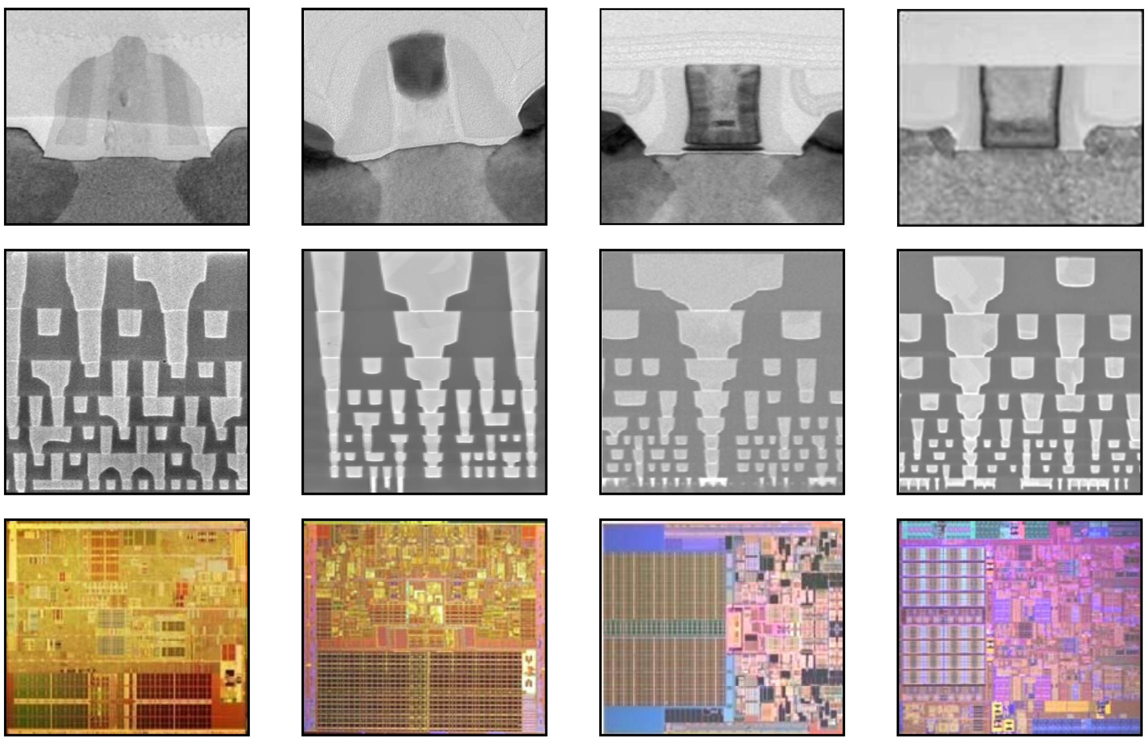
32nm – WIDE
0.171 μm^2

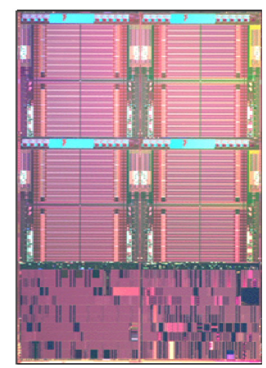


22nm – WIDE
0.092 μm^2

90 nm	65 nm	45 nm	32 nm	22 nm
2003	2005	2007	2009	2011 *projected*

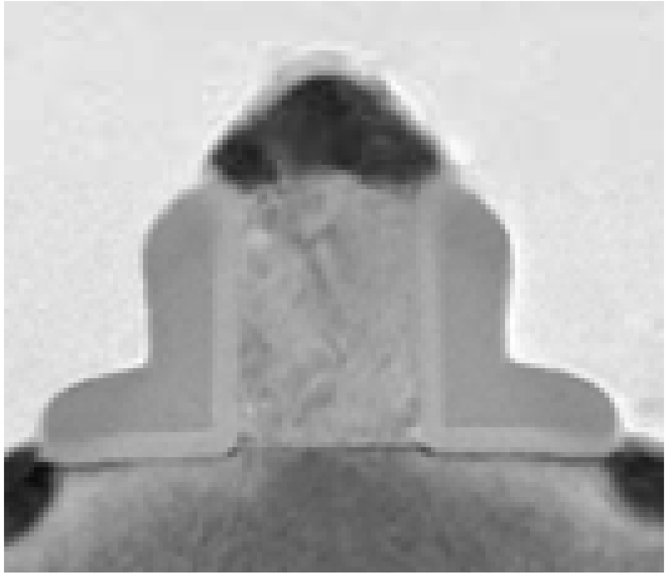
90: 7
65: 8
45: 9
32: 9

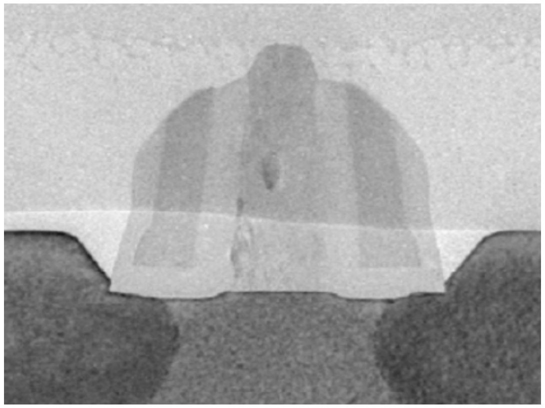


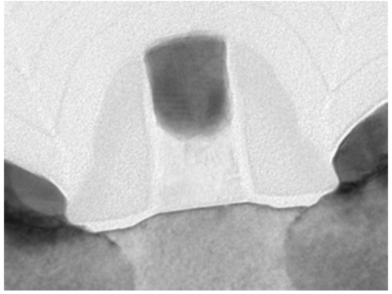


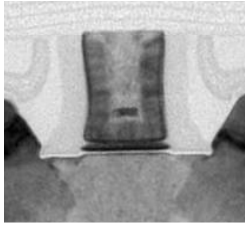
Changes in Scaling

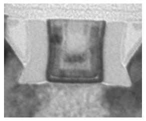
THEN	NOW
• Scaling drove down cost	• Scaling drives down cost
• Scaling drove performance	• Materials drive performance
• Performance constrained	• Power constrained
• Active power dominates	• Standby power dominates
• Independent design-process	• Collaborative design-process


130nm

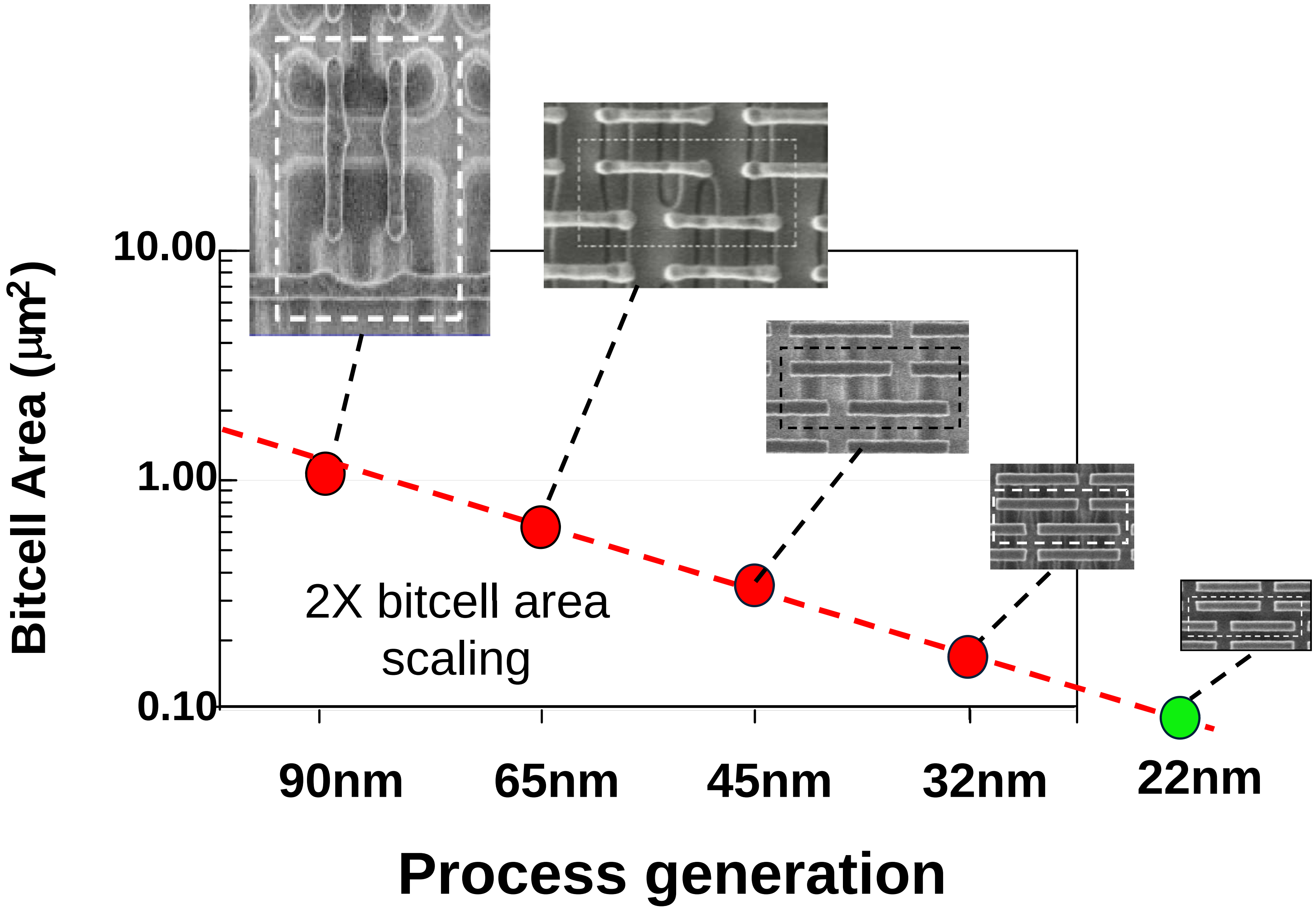

90nm


65nm


45nm


32nm

Consistent SRAM Density Scaling



K. Zhang, ISCC, 2009; M. Bohr IDF 2010

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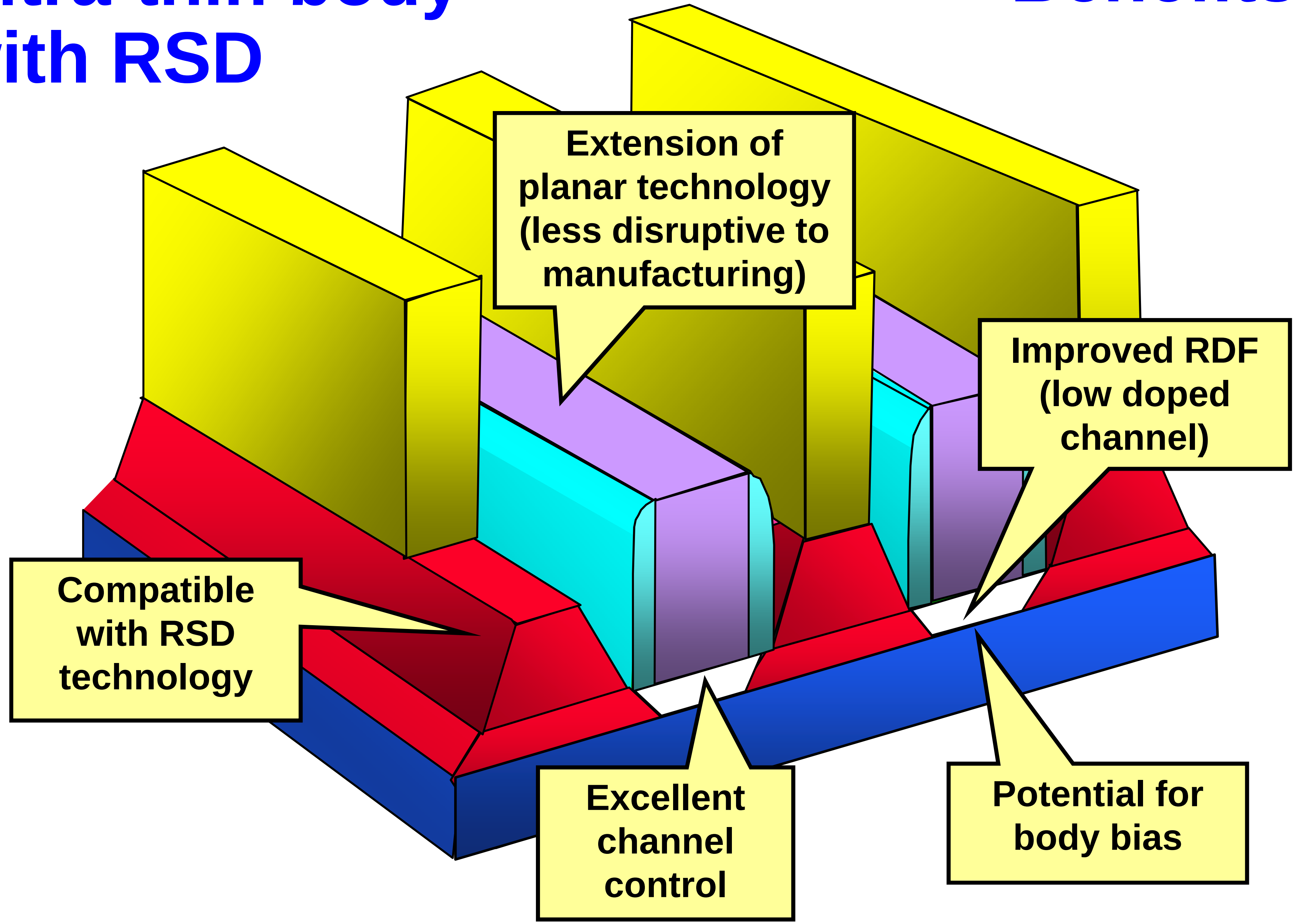
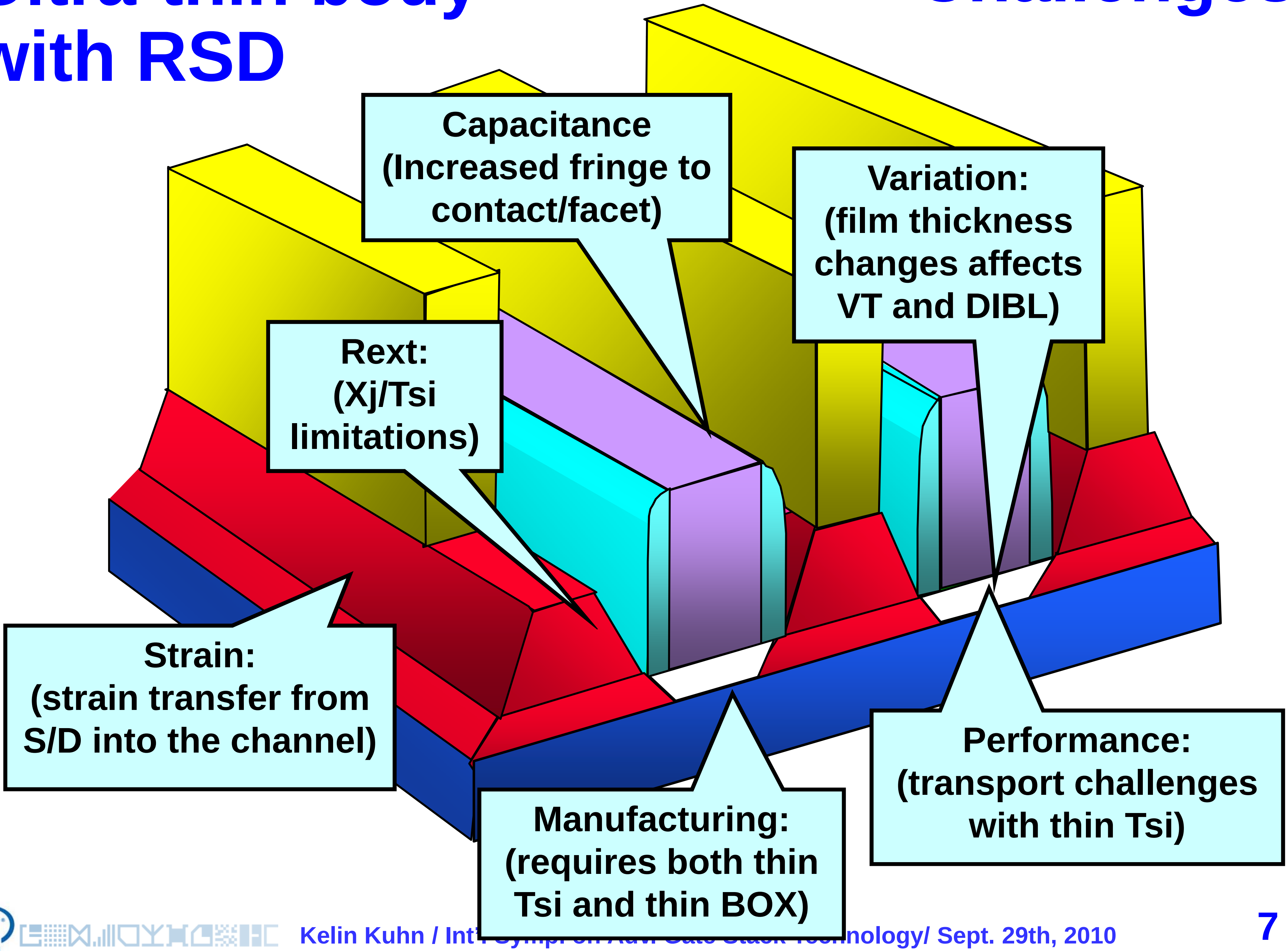
Ultra-thin body with RSD

Benefits



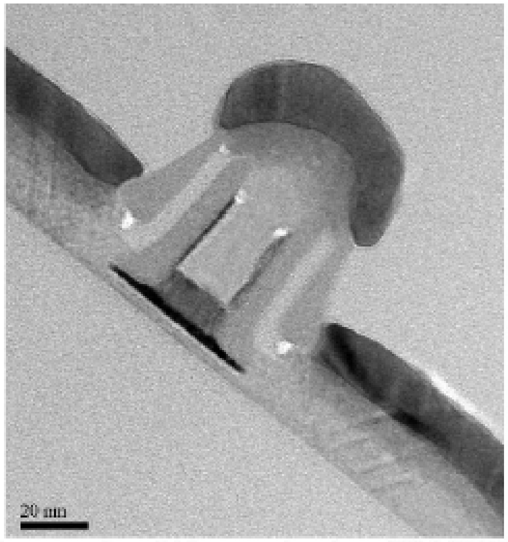
Ultra-thin body with RSD

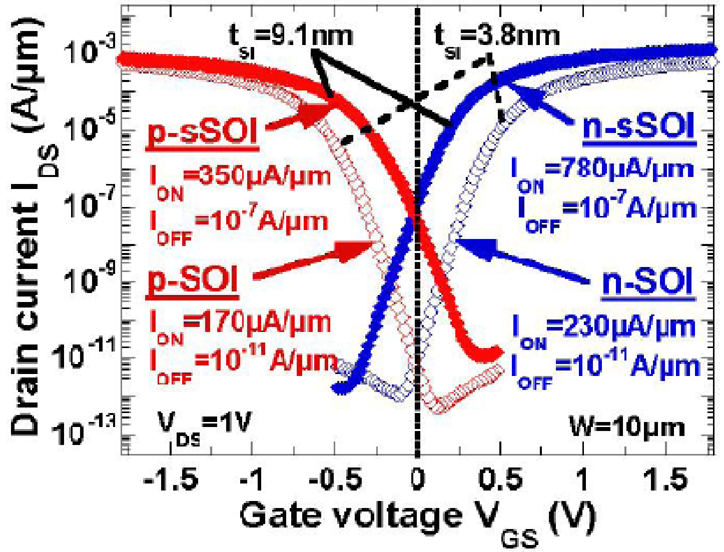
Challenges

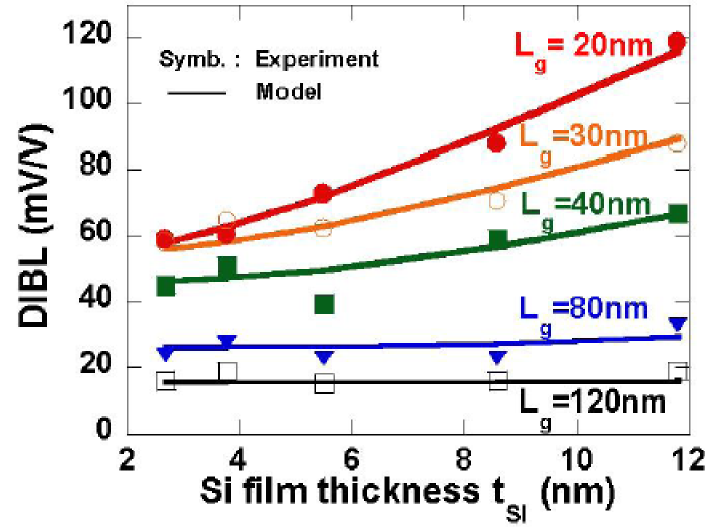


Ultra-thin body

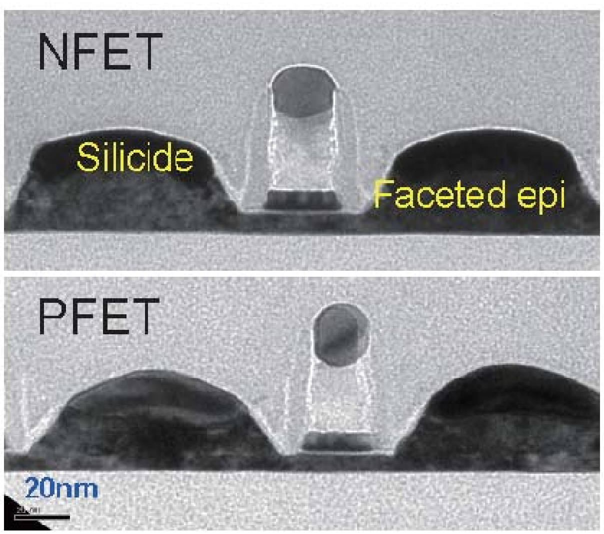
Barral – CEA-LETI / L2MP / SOITEC – IEDM 2007

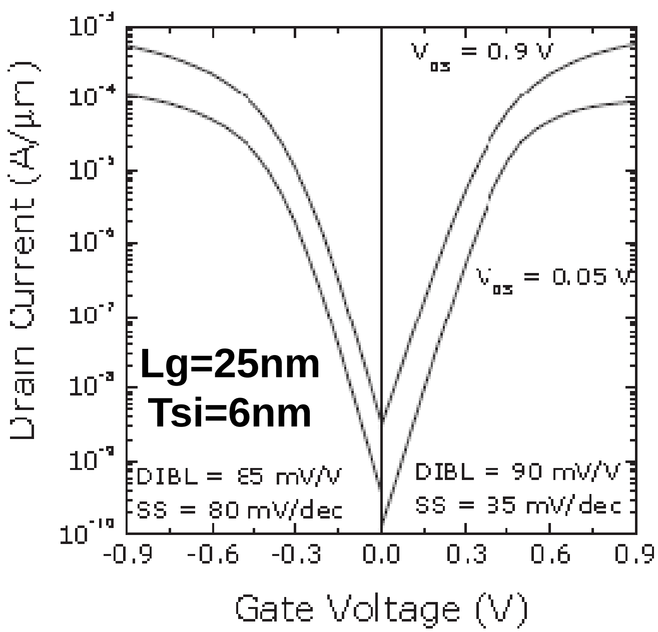


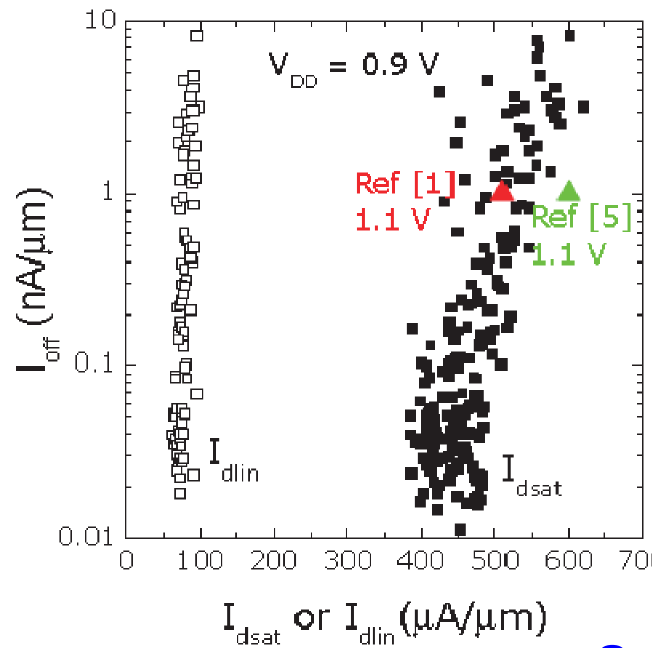




Cheng – IBM – VLSI 2009

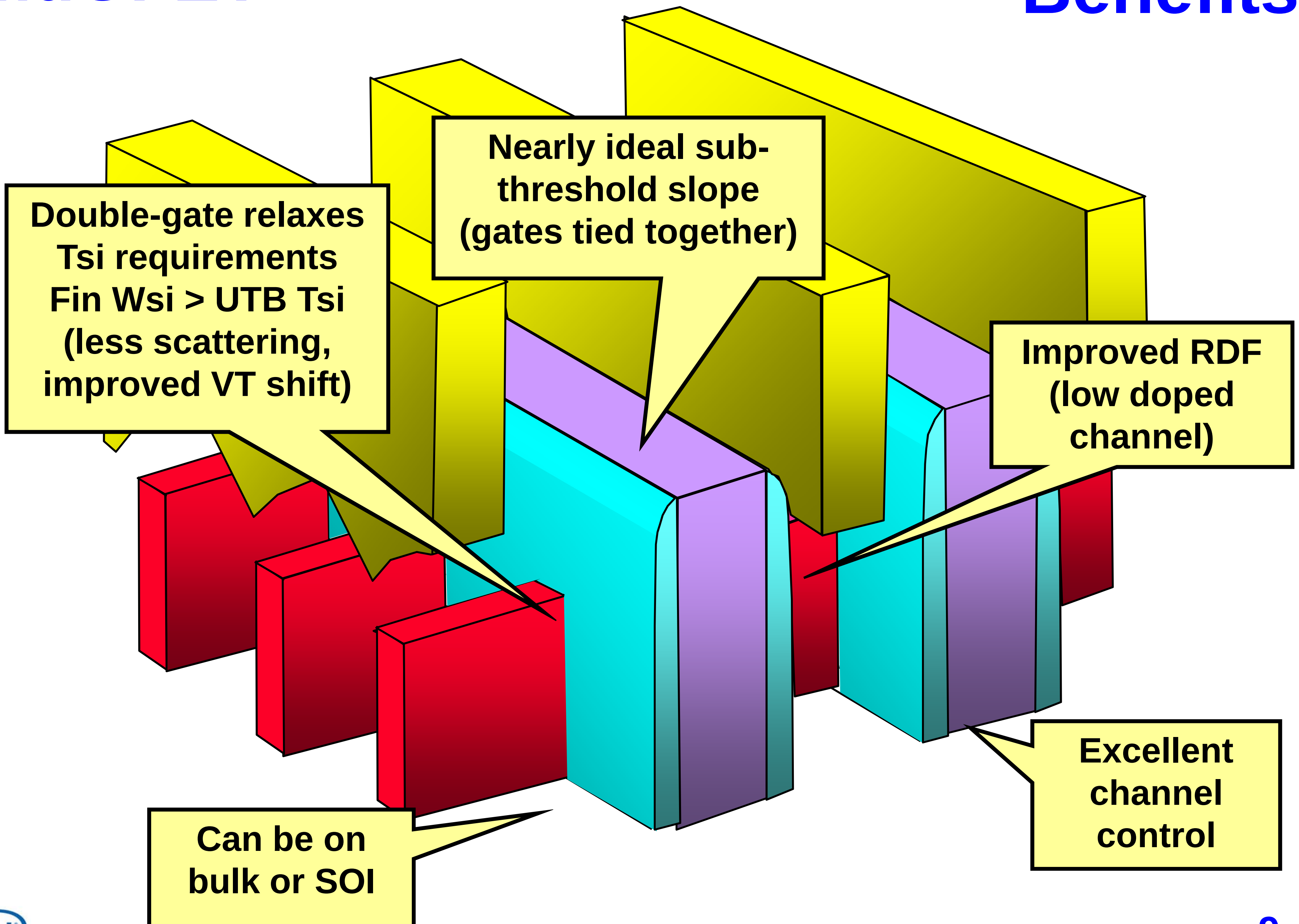






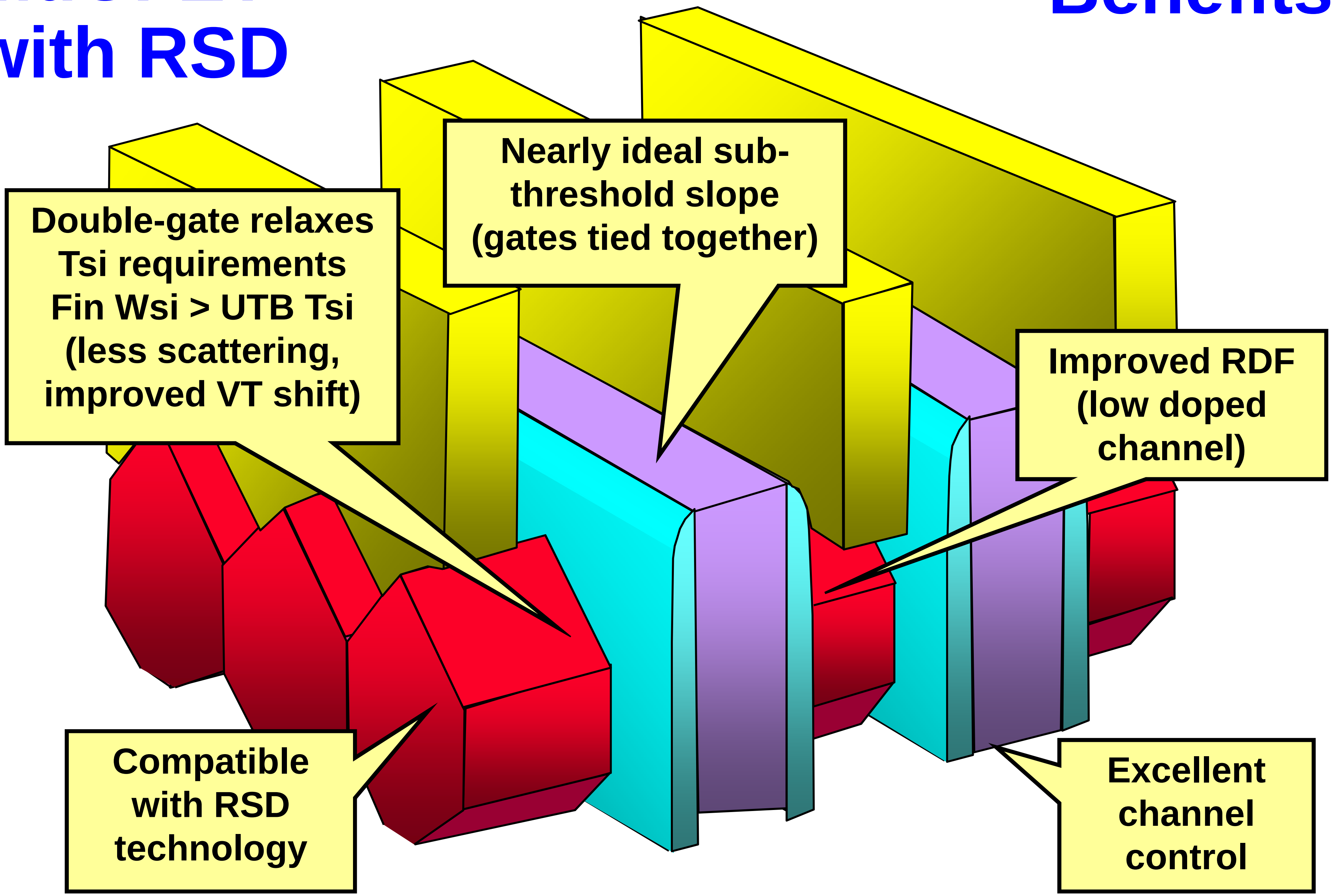
MuGFET

Benefits



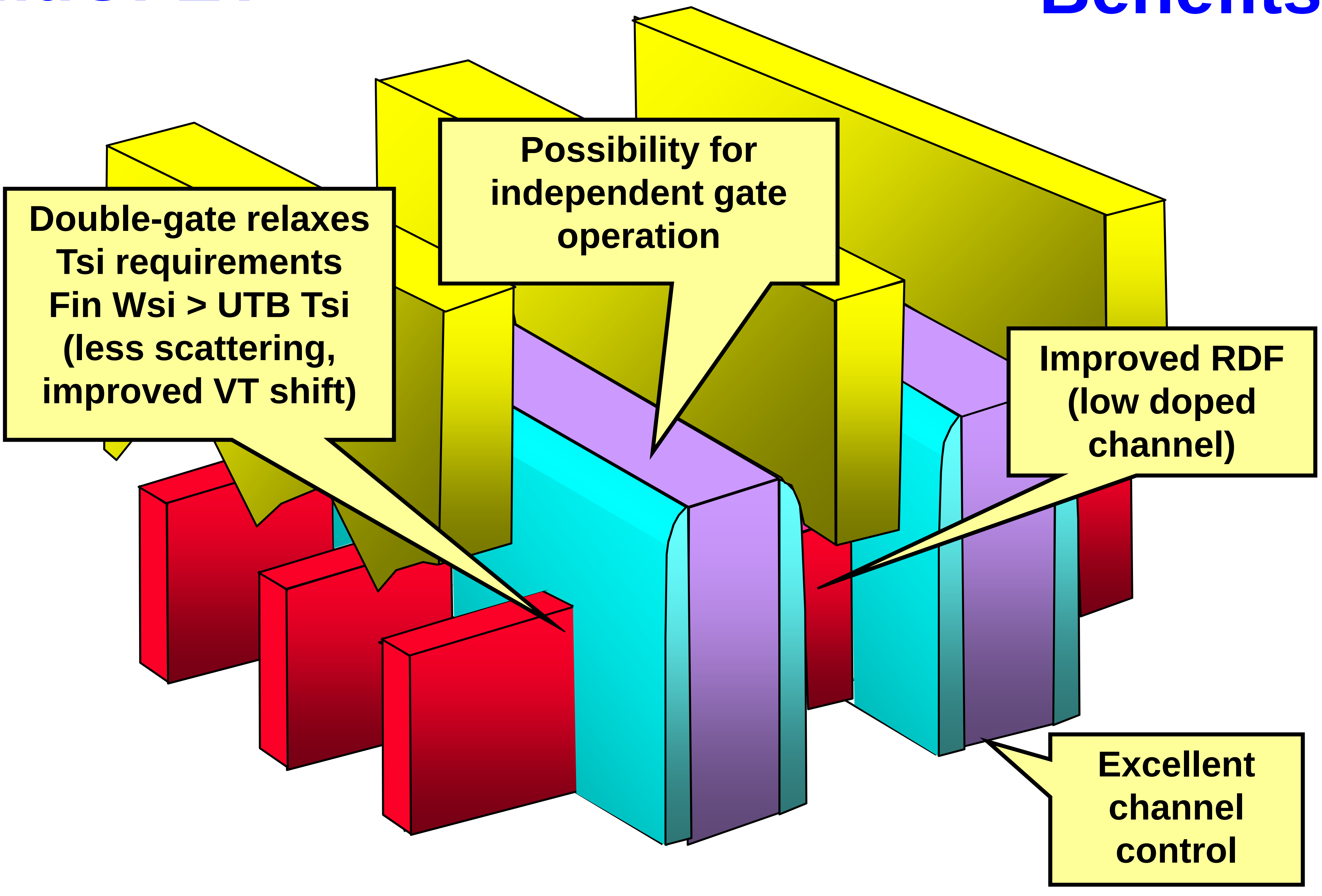
MuGFET with RSD

Benefits

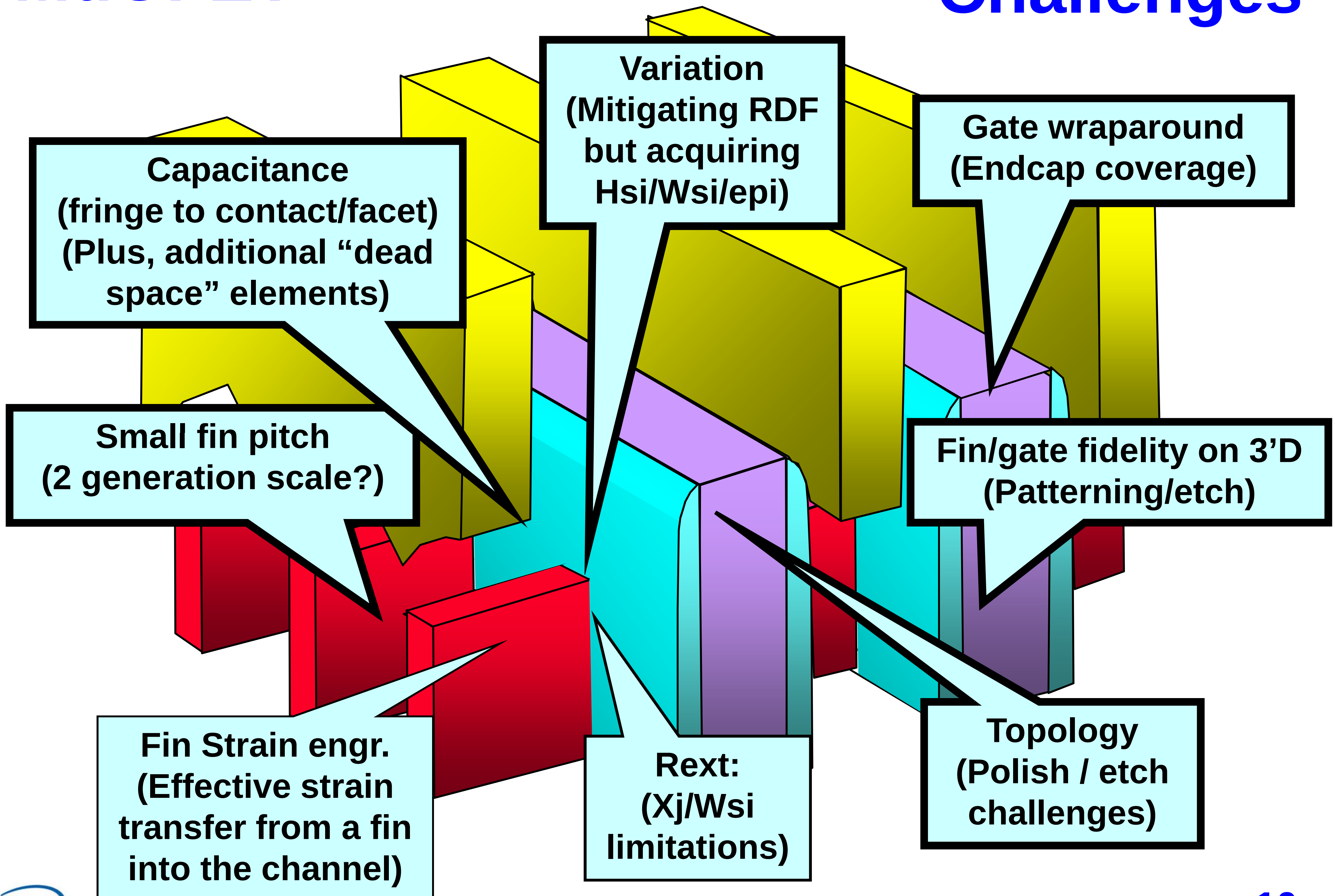


MuGFET

Benefits

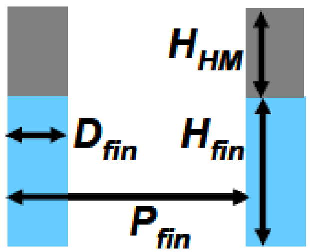


MuGFET Challenges

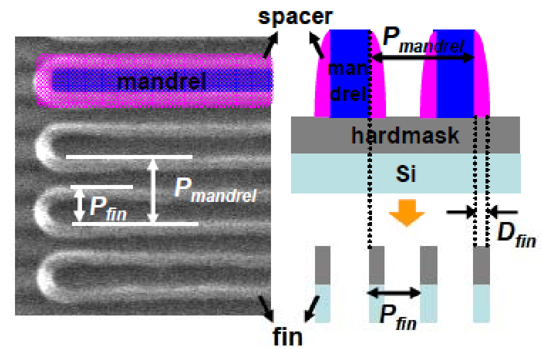


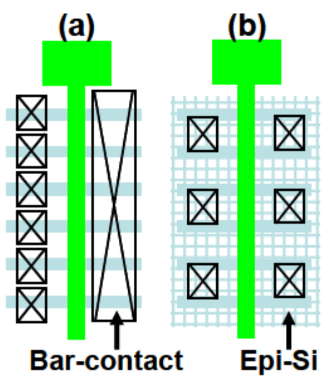
Kawasaki – Toshiba / IBM – IEDM 2009

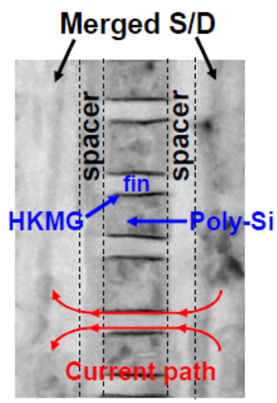
MuGFET

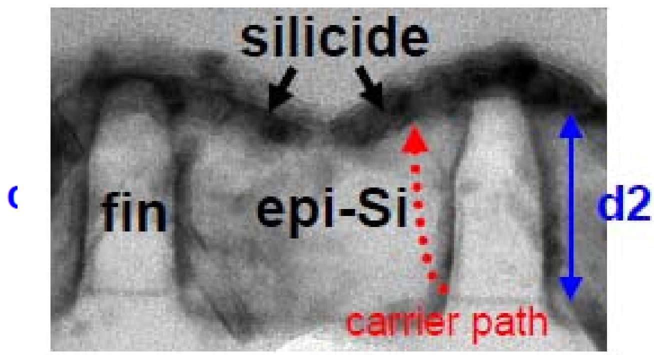


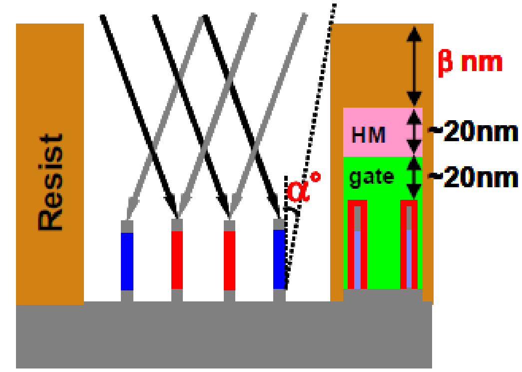
Year of production	2015	2018	2021
node (nm)	22	16	11
P_{fin} (nm)	40	28	21
D_{fin} (nm)	12	8	6
H_{fin} (nm)	28	20	15
SRAM cell size (μm^2)	0.063	0.03	0.015
L_g at cell (nm)	24	16	12

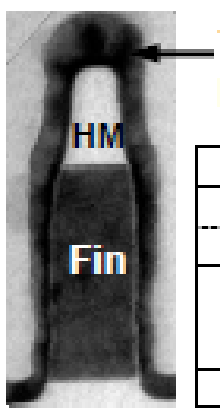






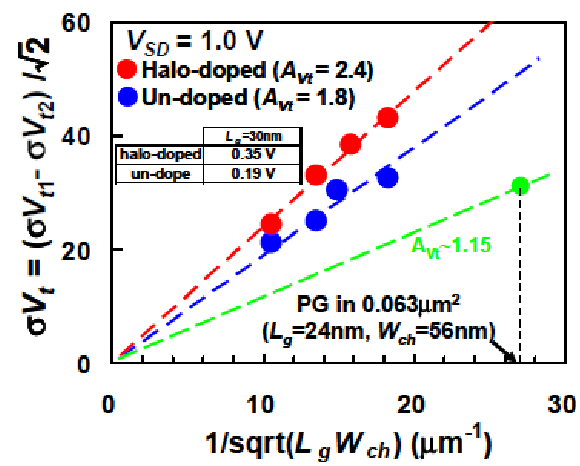




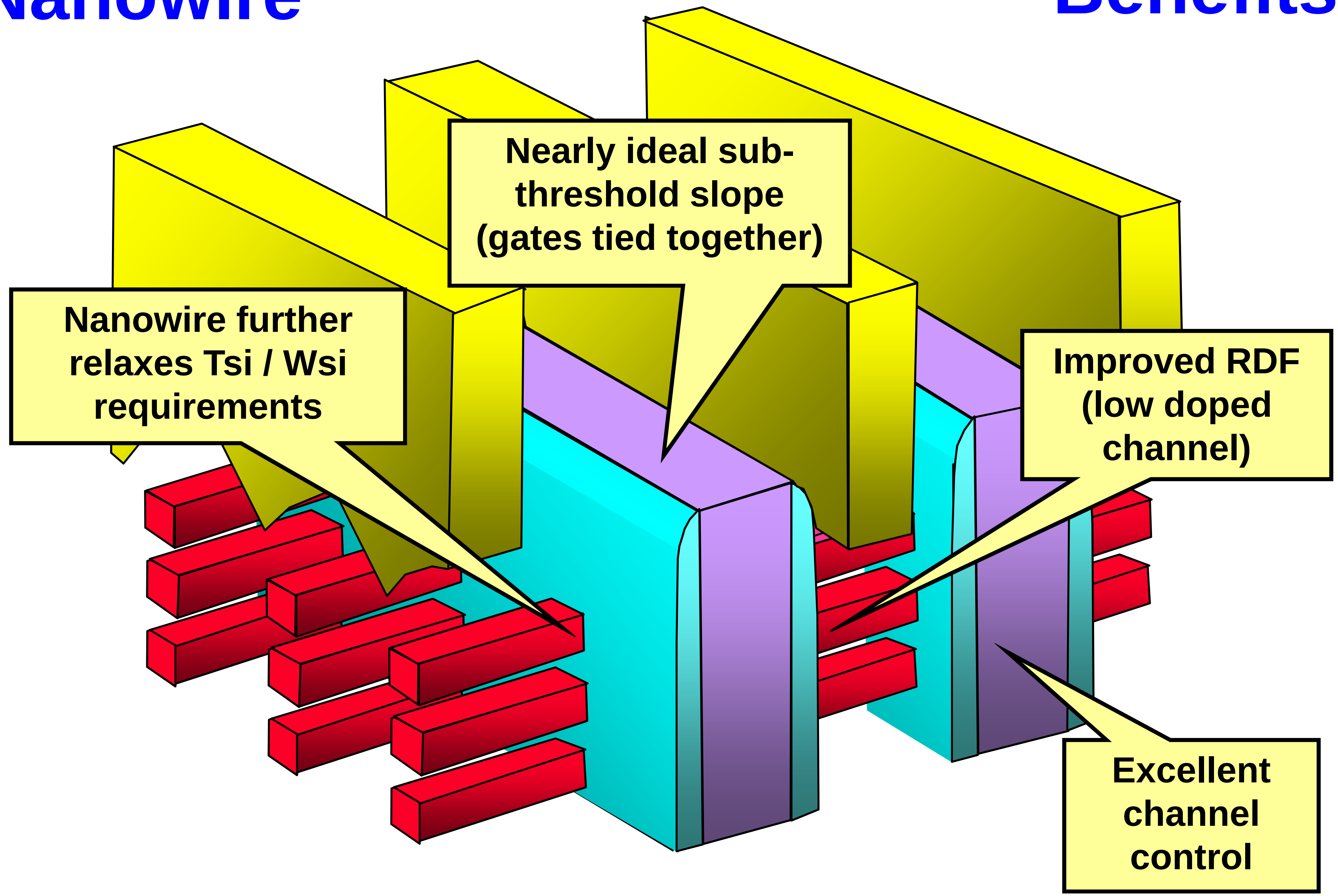


The thickness of HKMG should be uniform along fin height.

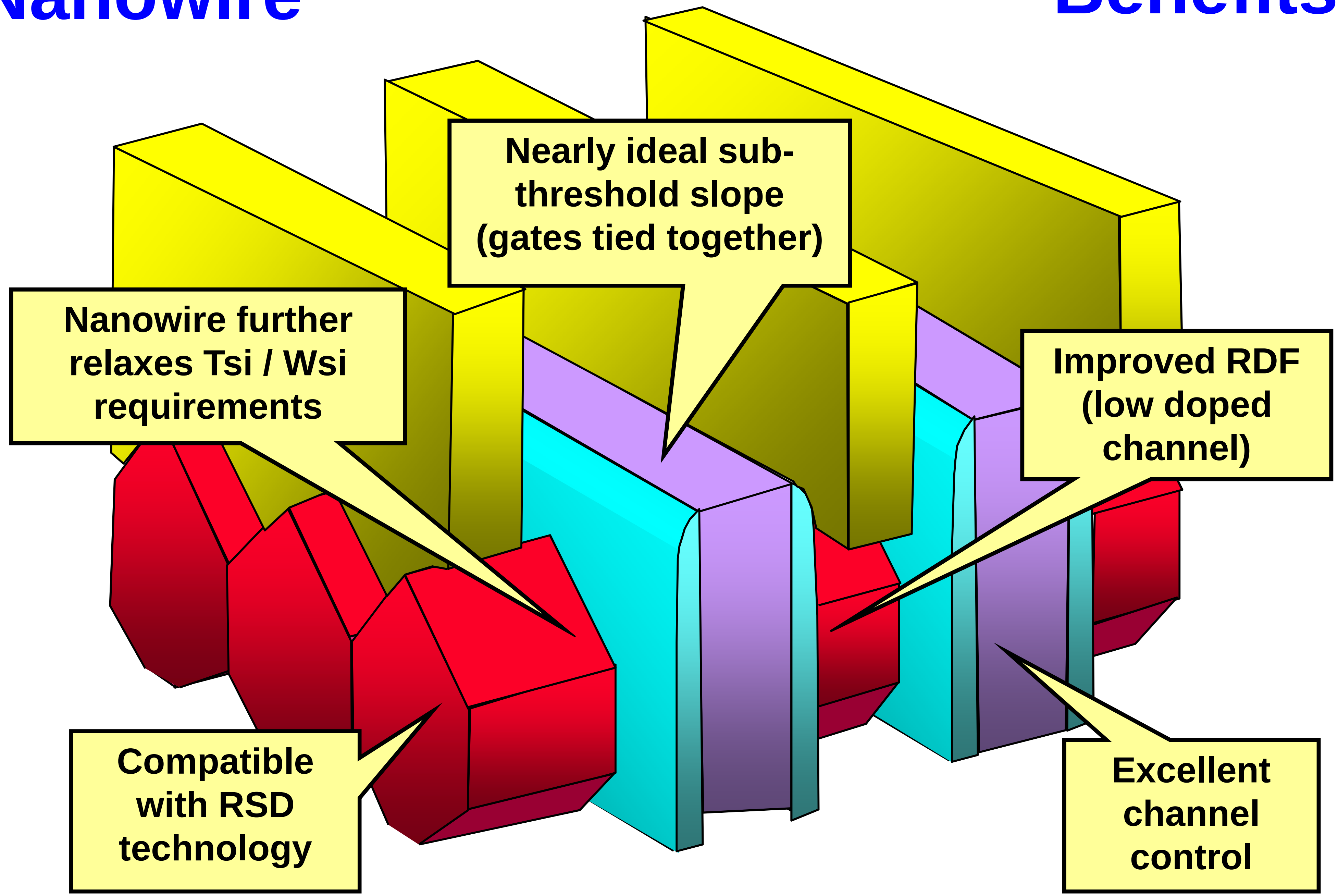
source of σV_t	origin
T_{ox} variation	non-uniform thickness of HK
ε_{ox} variation	non-uniform composition of HK
WF avriation	non-uniformity of MG
	grain size variation
	multi-surface oritations
charges	traps and states



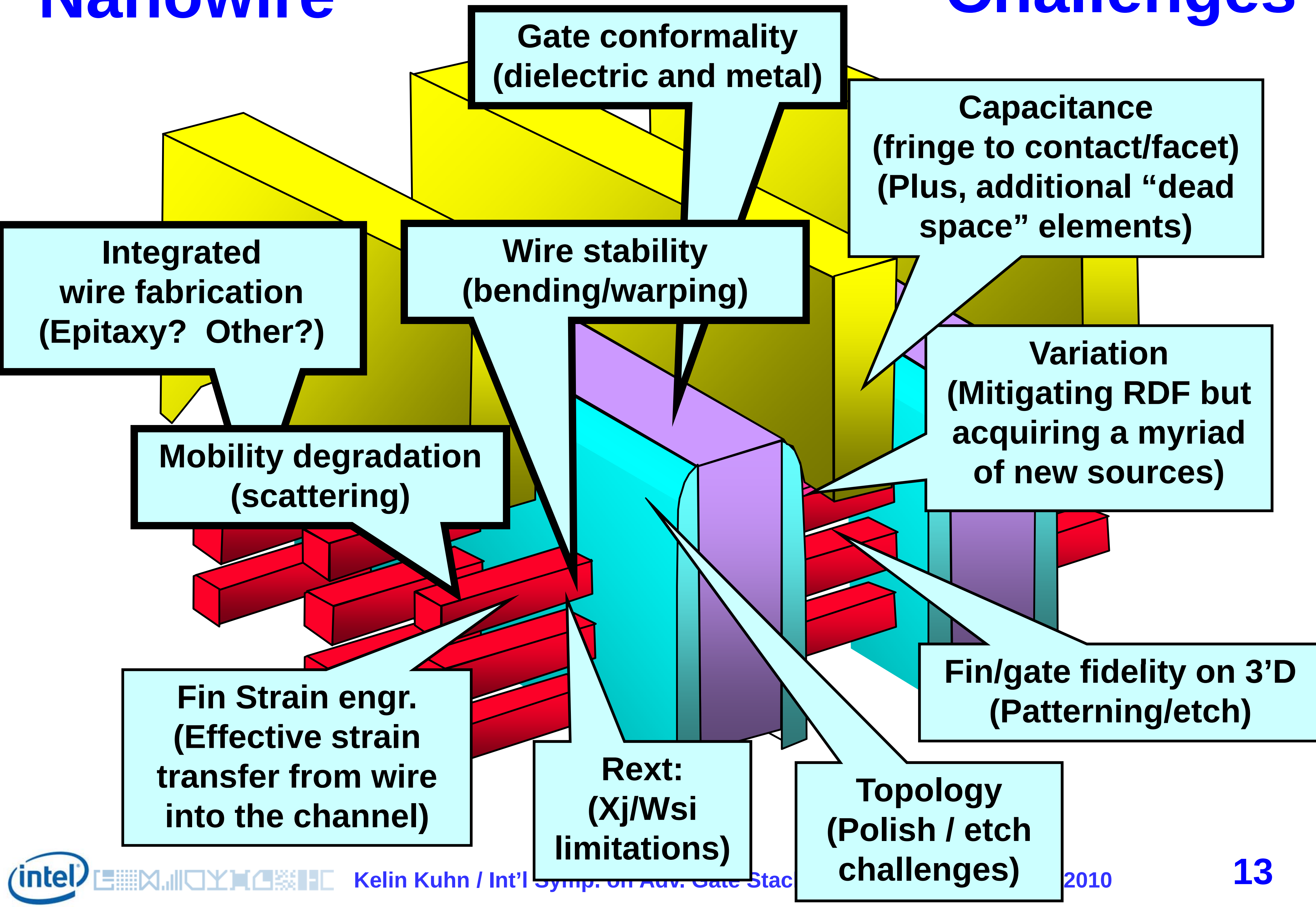
Nanowire Benefits



Nanowire Benefits

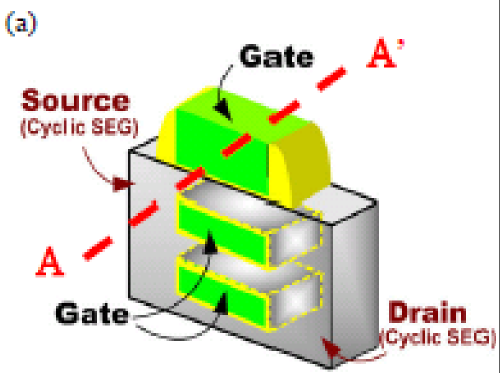


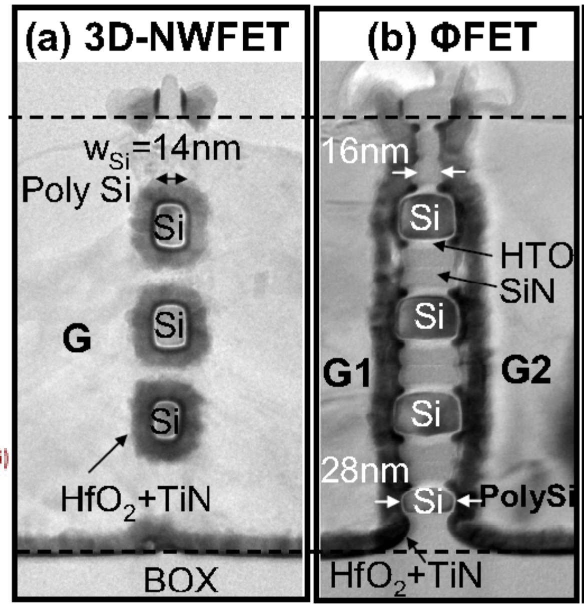
Nanowire Challenges

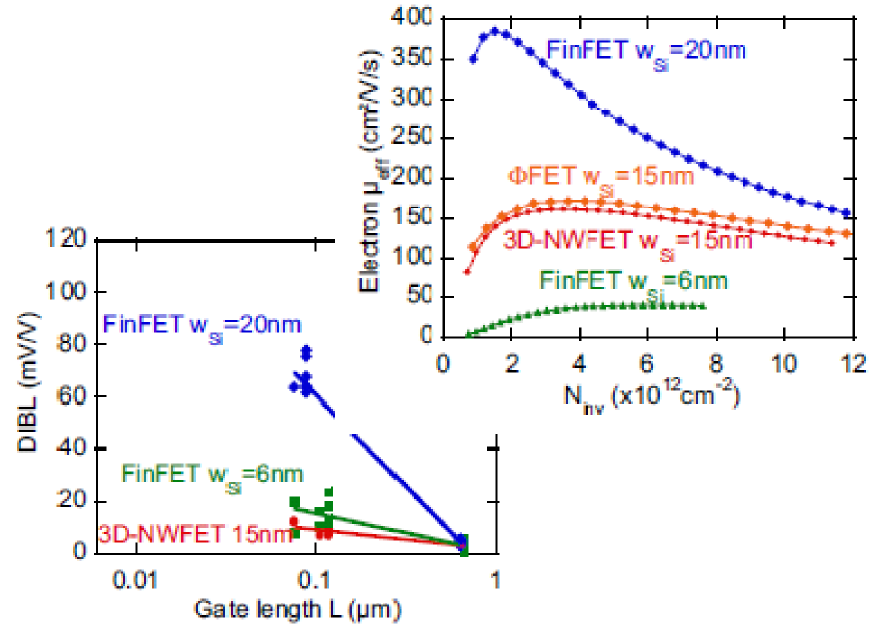


Nanowire FETs

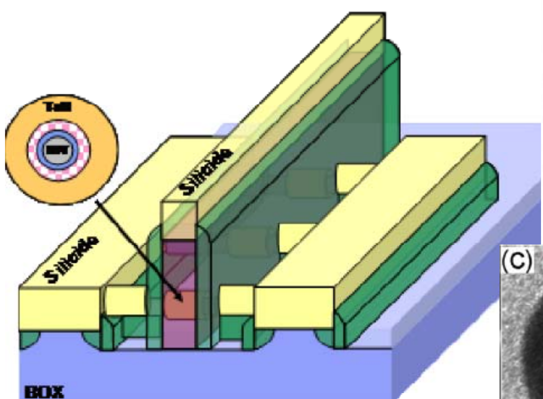
Dupre – CEA-LETI – IEDM 2008

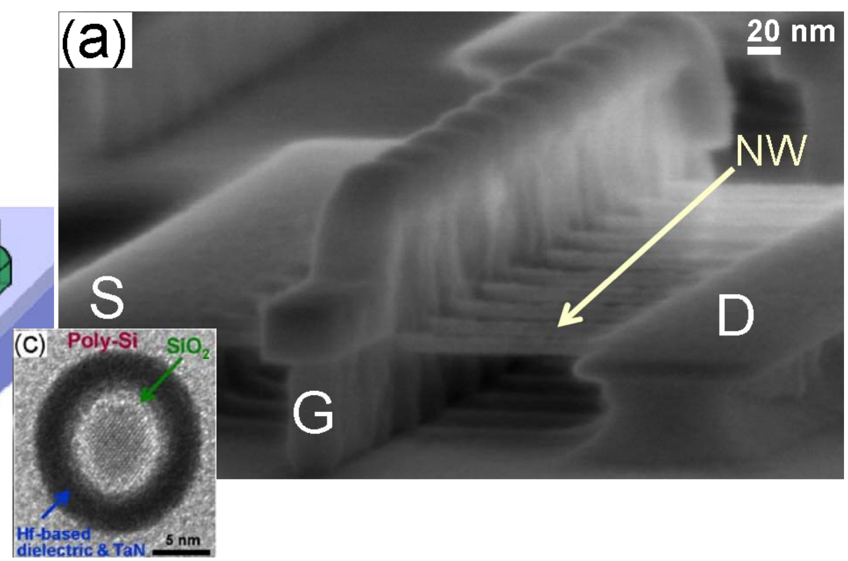


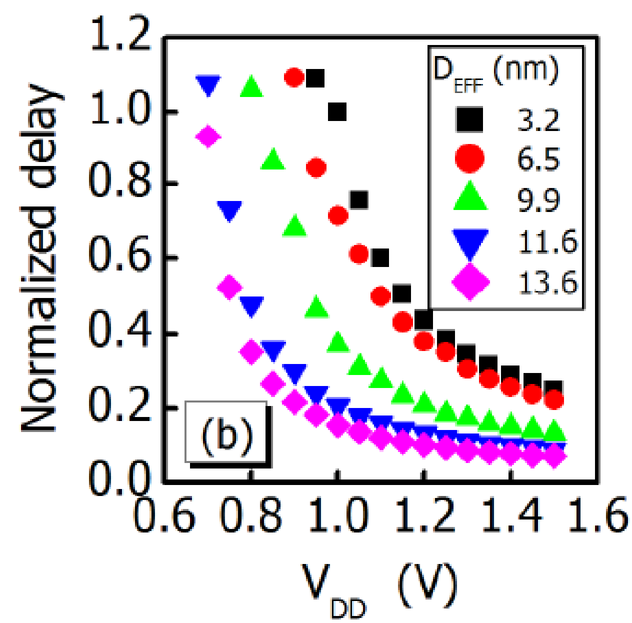




Bangsaruntip – IBM – IEDM 2009

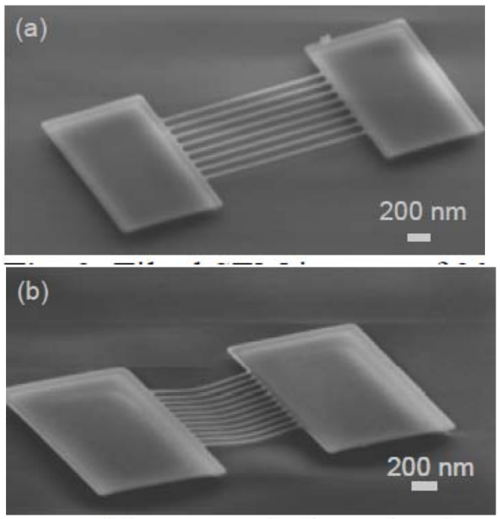


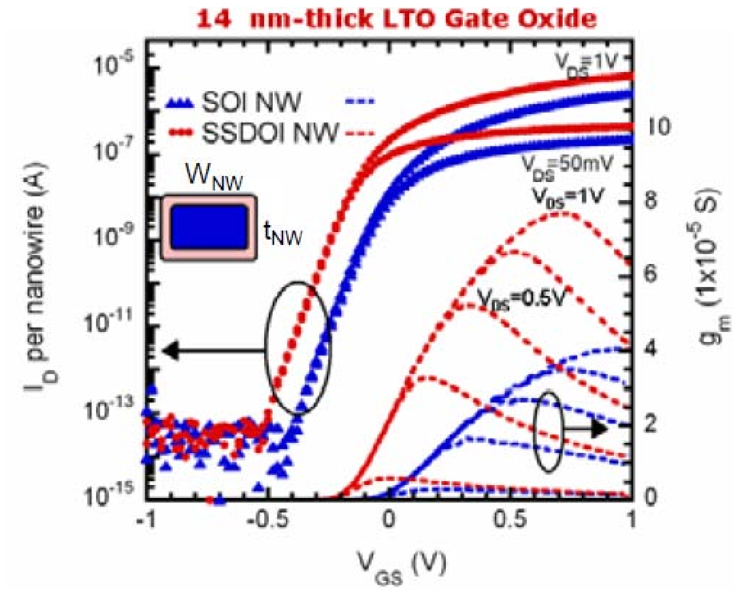


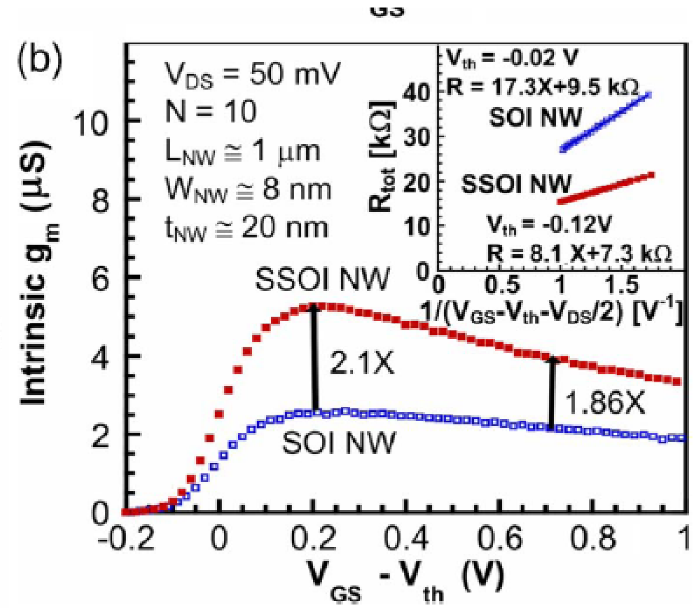


Nanowire FETs

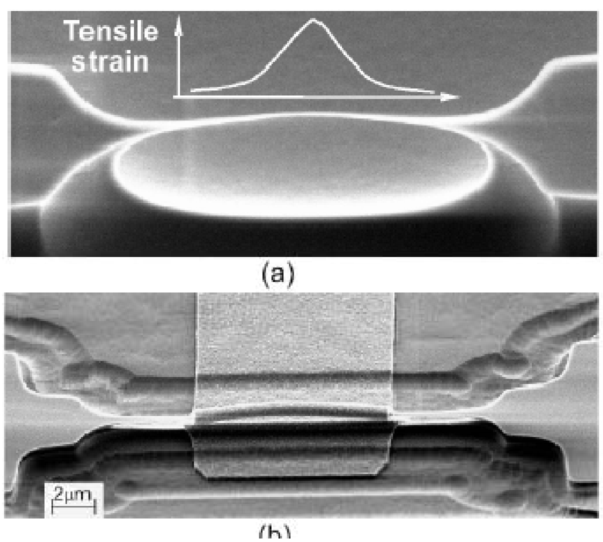
Hashemi/Hoyt – MIT
IEDM 2008 EDL/ESSDRC 2009

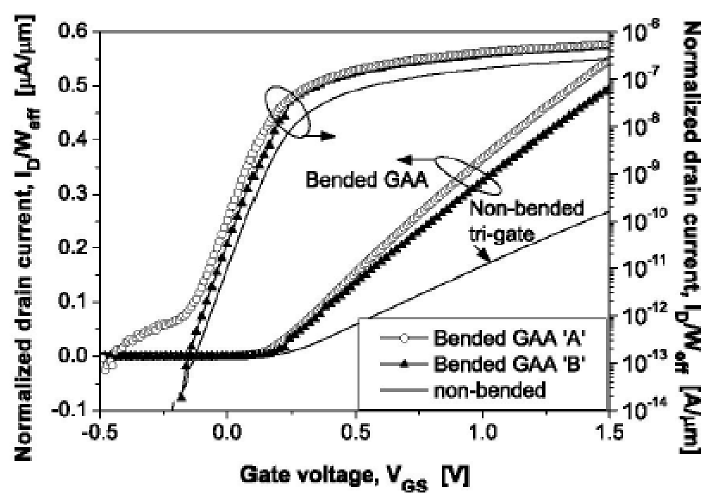


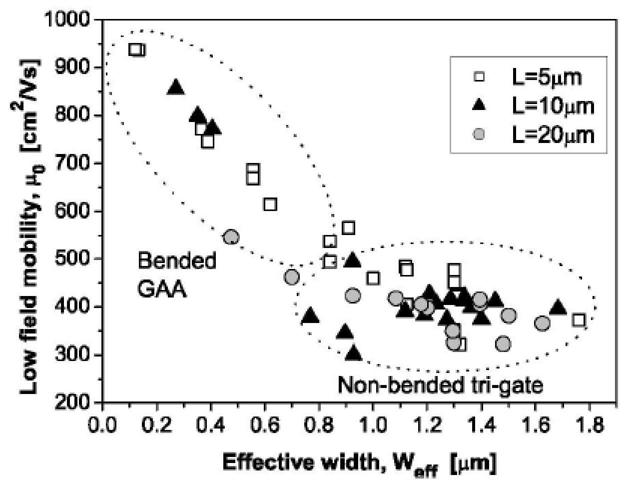




Moselund – Ecole Polytechnique, Switzerland
IEDM 2007

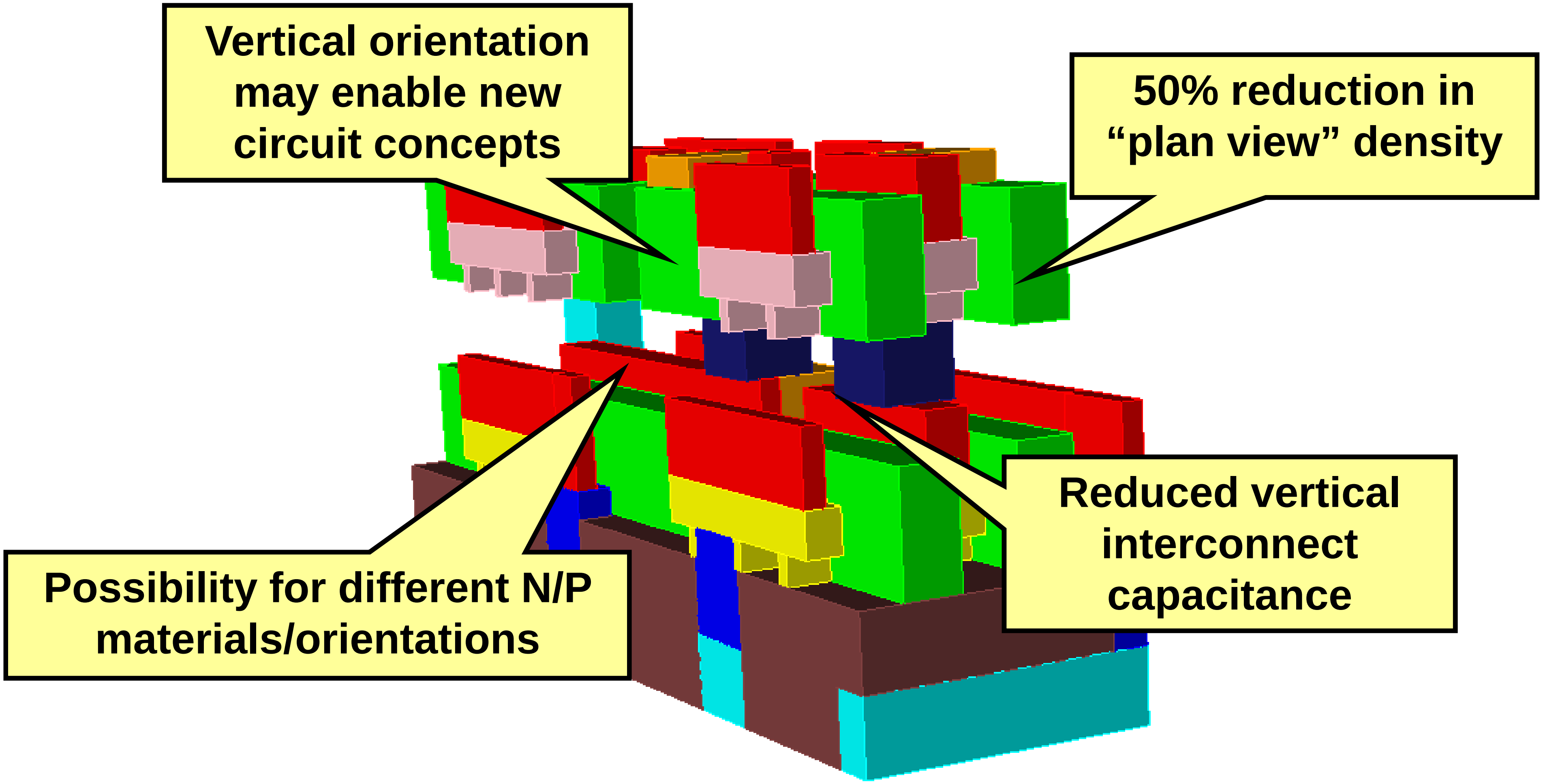




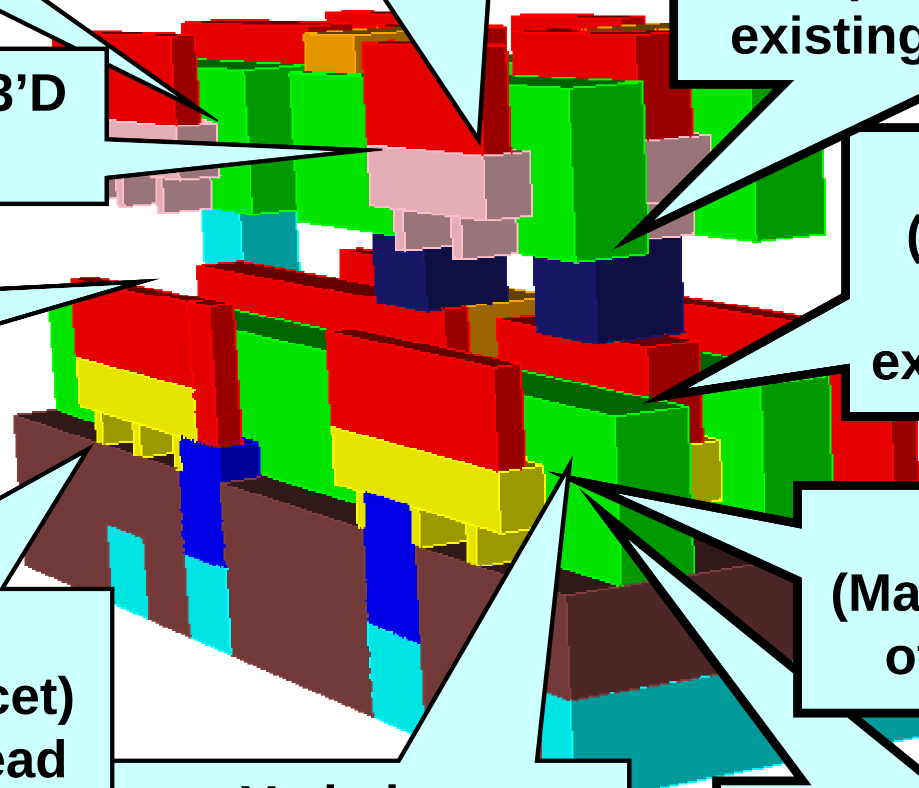


Vertical Architectures

Benefits



Vertical Architectures Challenges



Rext: (Xj/Wsi limitations)

Gate conformality (dielectric and metal)

Thermal processing (Top layer may need to be processed over existing bottom layer)

Fin/gate fidelity on 3'D (Patterning/etch)

Contacts (Diffusion-diffusion, Gate-gate contacts extremely challenging)

Topology (Polish / etch challenges)

Lithography (May double the number of FE critical layers)

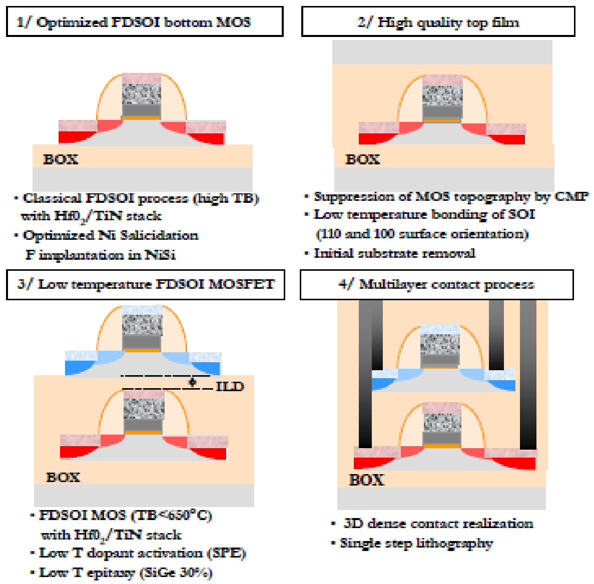
Capacitance (fringe to contact/facet) (Plus, additional "dead space" elements)

Variation (Mitigating RDF but acquiring a myriad of new sources)

Strain engineering (more challenging than single layer)

Batude – CEA LETI - IEDM 2009 – stacked 110/100

Vertical



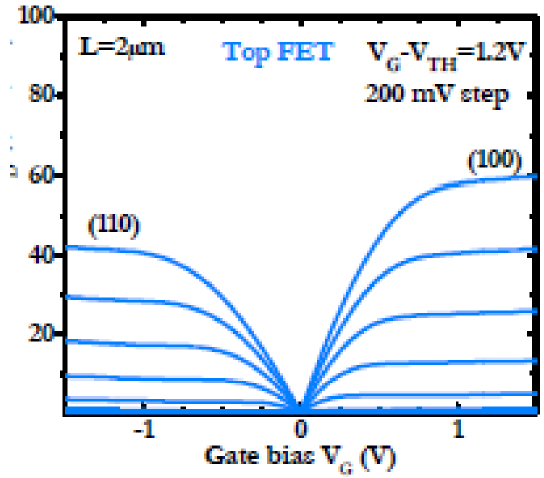


Fig.15: I_D-V_D characteristics of top FET

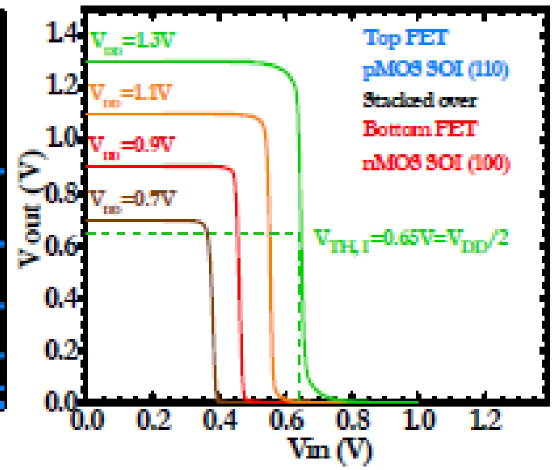
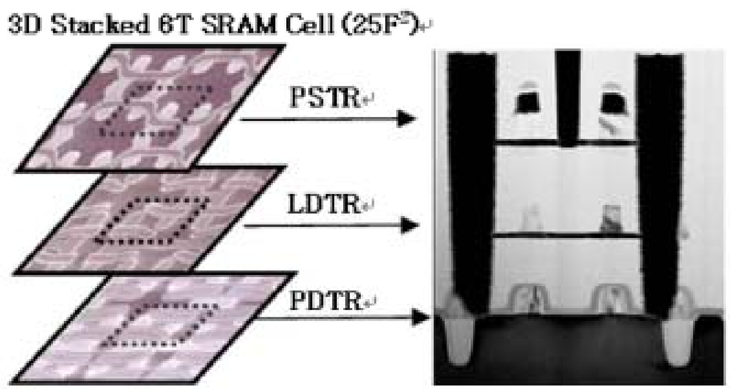
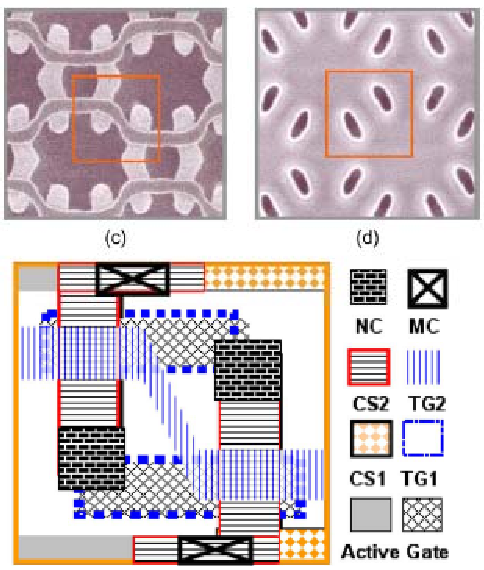
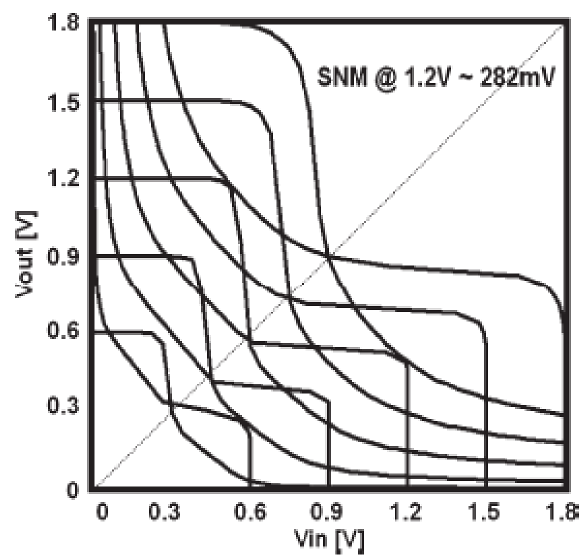


Fig.16: Transfer Voltage characteristic of an inverter: top SOI (110) pFET and bottom SOI (100) nFET

Jung – Samsung - IEEE TED 2010 – 3'D stacked 6T







TFET (Tunneling Field-Effect Transistor)

Principle of operation

- Band-to-band- tunneling through source barrier, modulated by gate field

Advantages

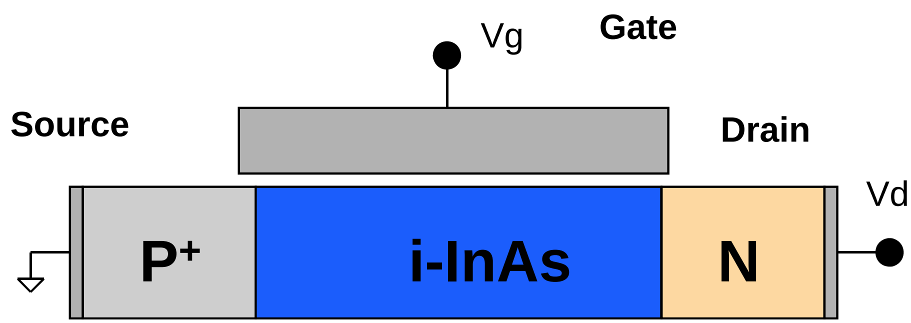
- Steep (< 60 mV/dec) sub-threshold slope
- Large Ion/Ioff ratio

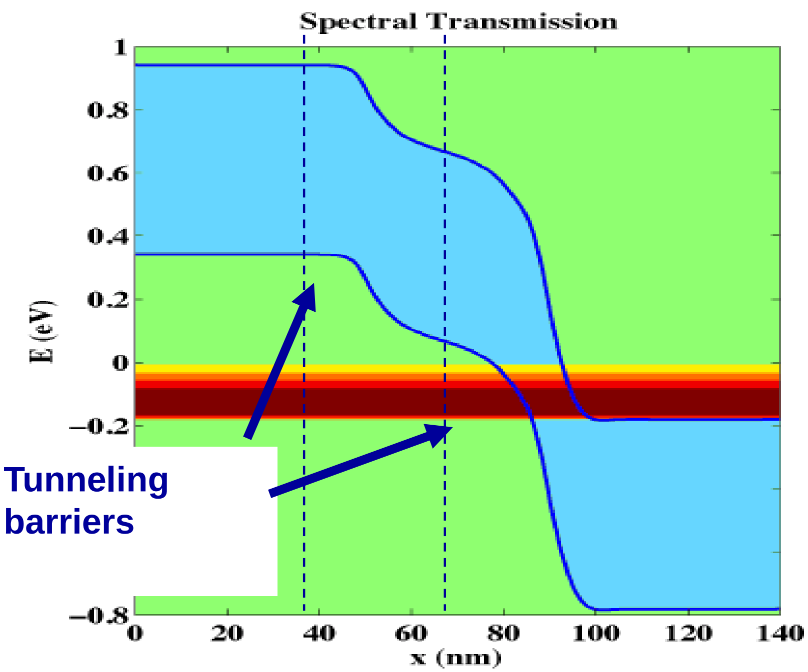
Disadvantages

- Low drive currents
- Ambipolar conduction
- Unidirectional conduction
- Potentially high hot-e$^-$ effects

Technology Intercept

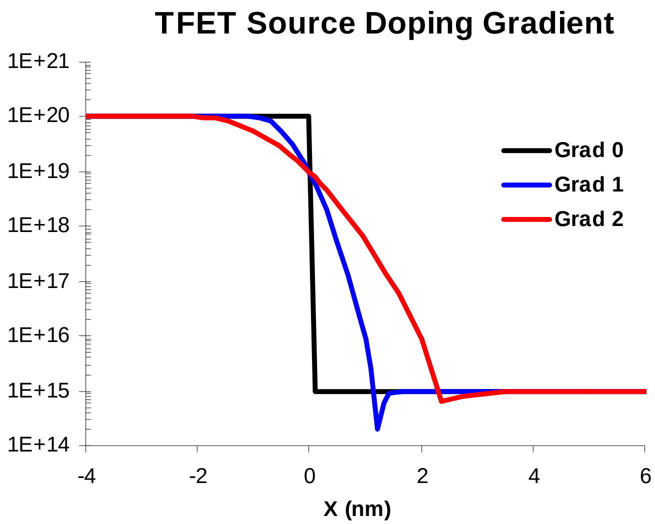
- Unlikely candidate for Si, Ge, or $Si_{1-x}Ge_x$ systems (drive currents too low)
- Need III-V band-gap engineering, perhaps with "broken-gap"

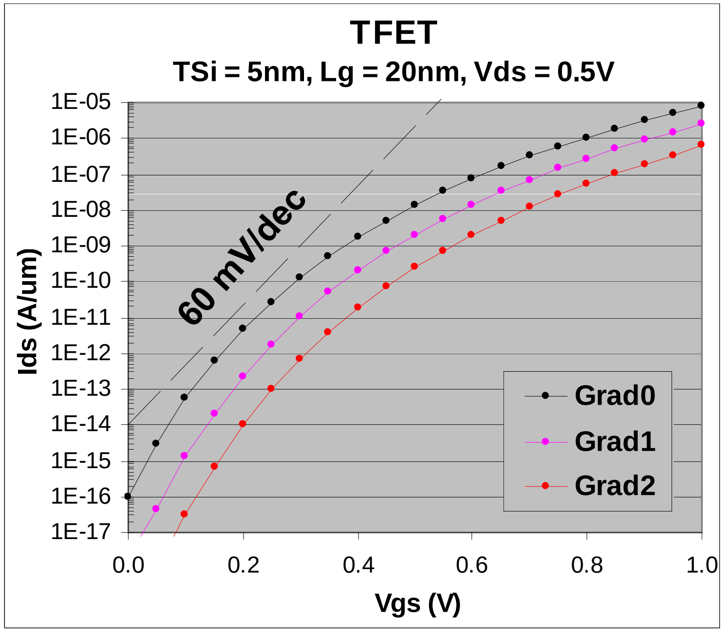




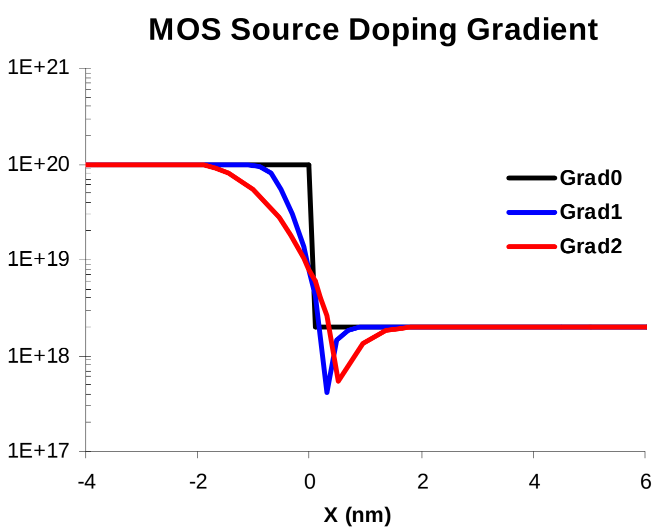
Courtsey M. Luisier (Purdue)
M. Luisier and G. Klimeck, EDL, 2009

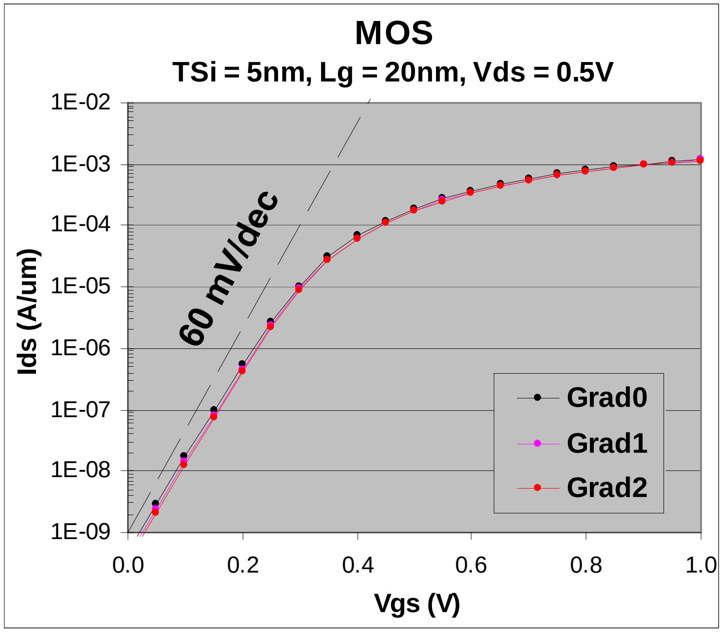
Sensitivity to Source Doping Variation





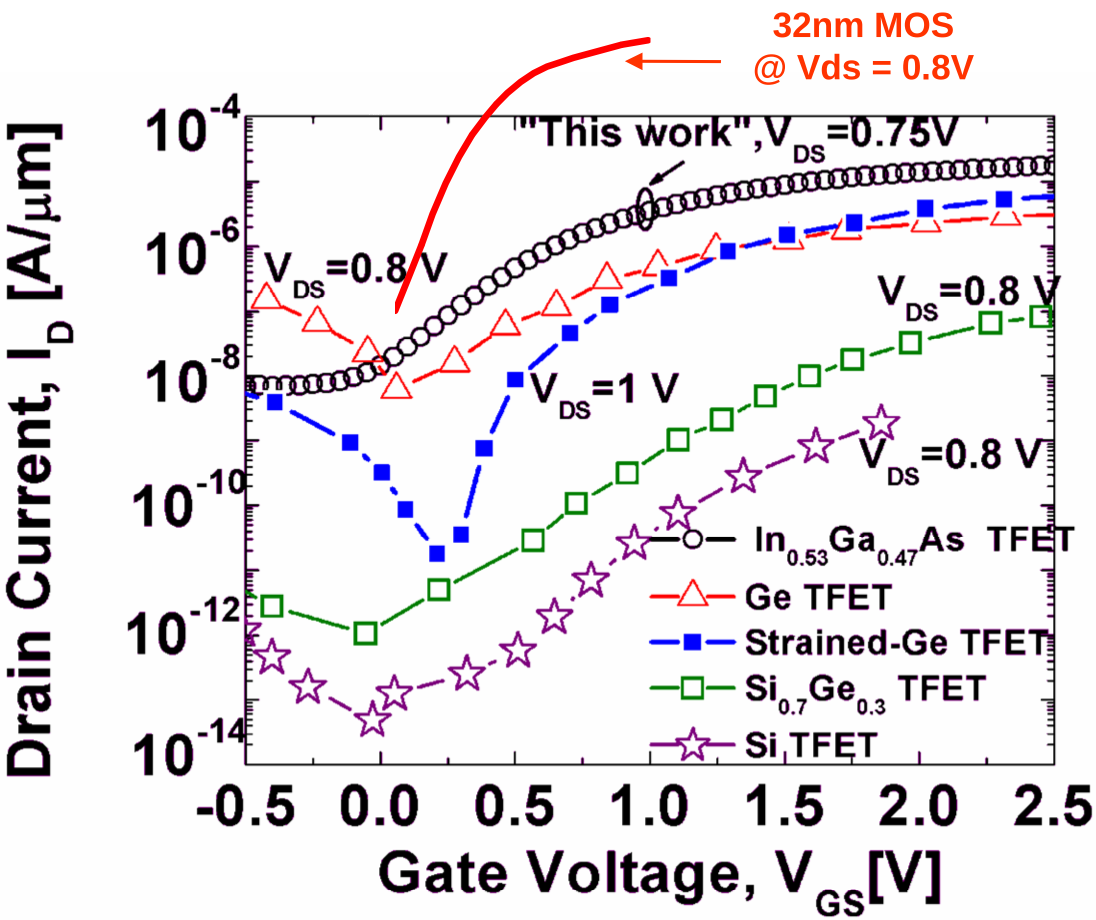
TFET behavior is very sensitive to the source doping "shape"





MOS behavior has little sensitive to the source doping "shape"

Best Demonstrated TFETs



S. Mookerjea et al., IEDM '09

- Still MUCH lower drive currents than conventional MOS
- Require band-gap engineering with hetero-junction δ layers
- Sub-threshold slope still poor

	Ref. [2]	Ref. [3]	Ref. [4]	[1]
SS (mV/dec)	52.8	42	~300	46
I_{ON} (μA/μm)	12.1	0.01	1E-4	1.2
I_{ON}/I_{OFF}	1E4	1E4	1E2	7E7

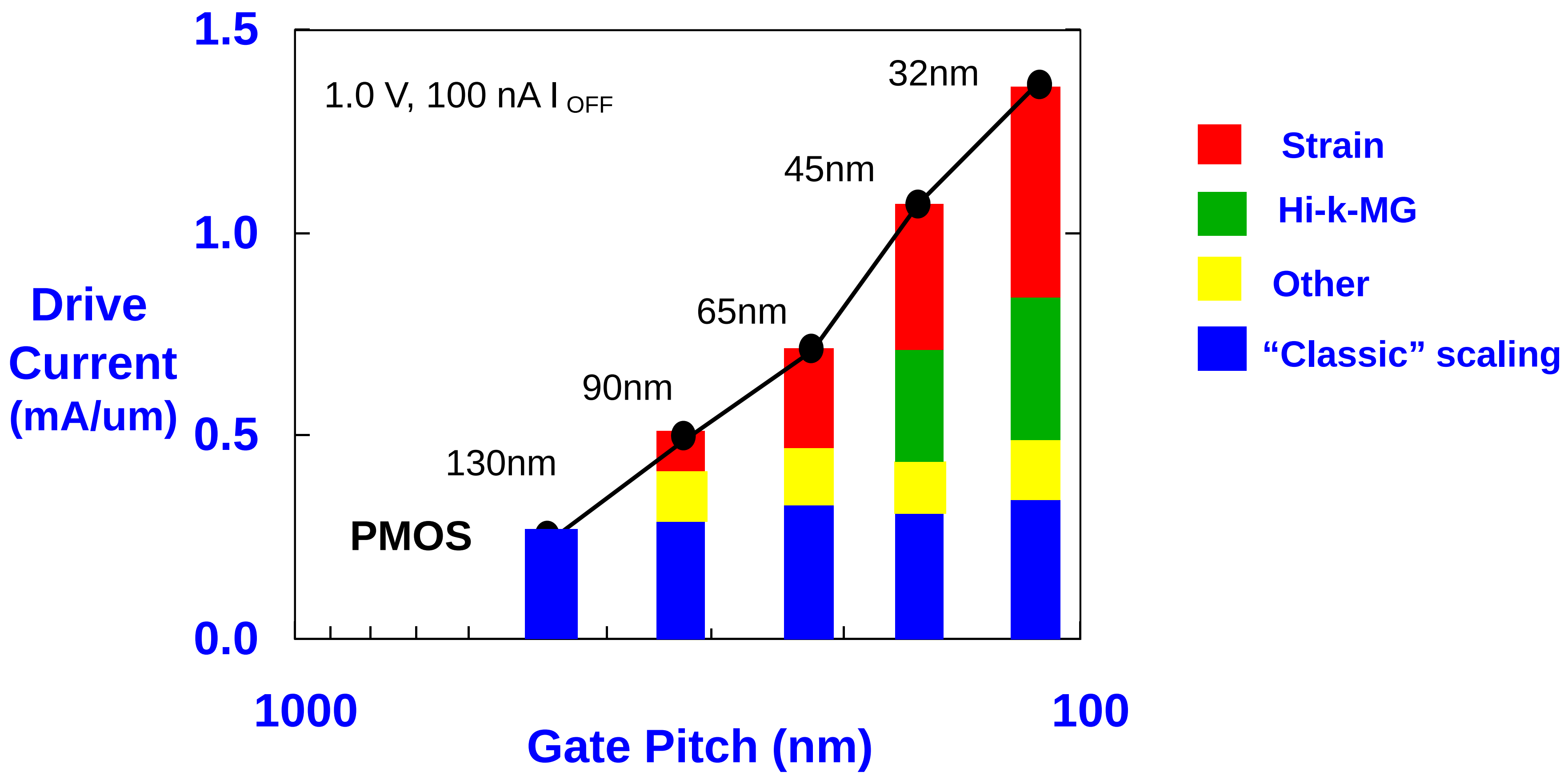
Table. I. Comparison to reported silicon TFETs. ($V_{DS}=V_{GS}-V_{BTBT}=1.0V$)

[1] K. Jeon, et al., VLSI (11.4.1.-1) 2010
[2] W. Choi et al., IEEE-EDL vol.28, no.8, p.743 (2007)
[3] F. Mayer et al., IEDM Tech Dig., p.163 (2008)
[4] T. Krishnamohan et al., IEDM Tech Dig., p.947 (2008)

AGENDA

- Scaling
- Gate control
- Mobility
- Resistance
- Capacitance
- Summary

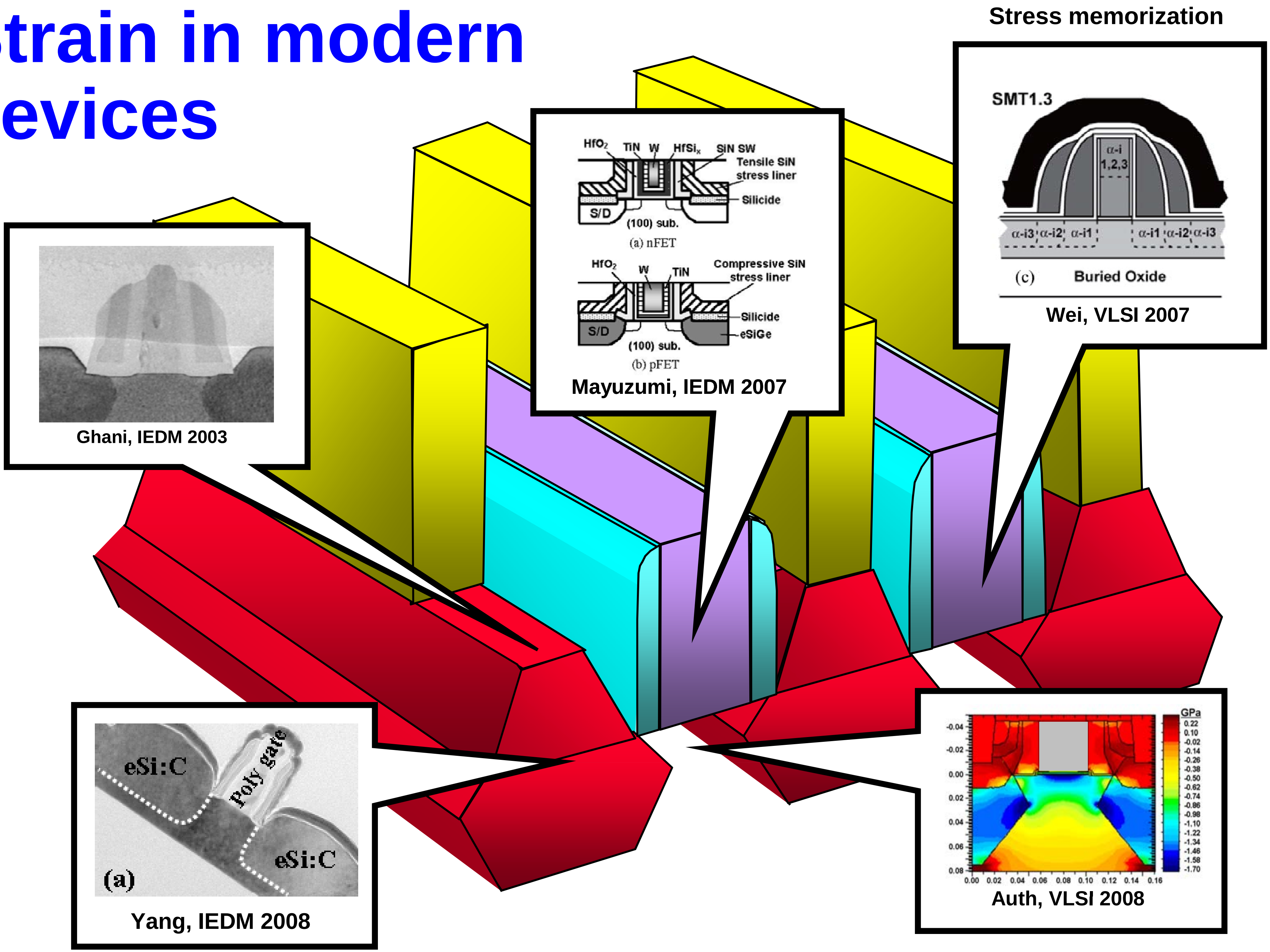
Transistor Performance Trend



Strain is a critical ingredient in modern transistor scaling

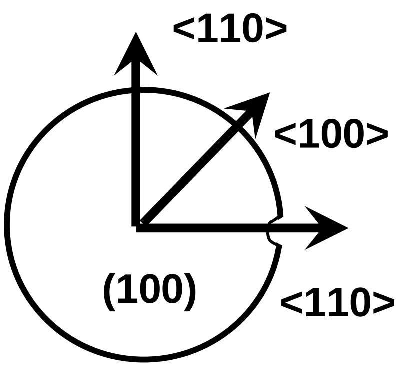
Strain was first introduced at 90nm, and its contribution has increased in each subsequent generation

Strain in modern devices



ORIENTATION

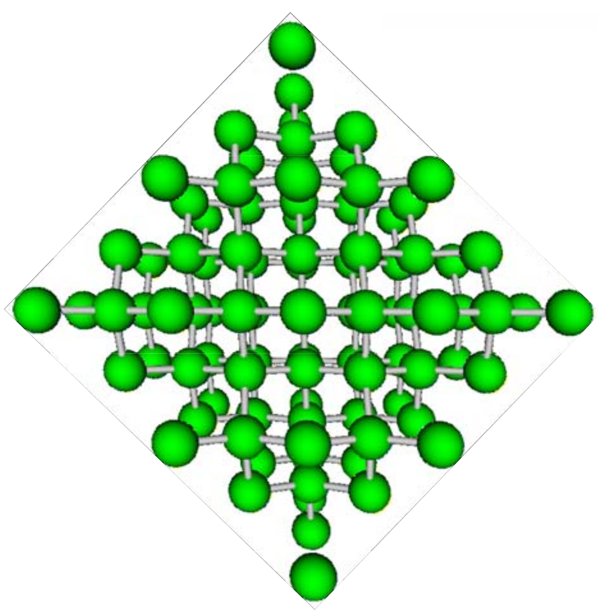
(100) surface – top down



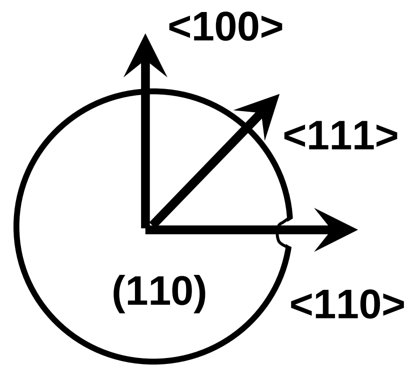
Standard wafer / direction
(100) Surface / <110> channel

(100) Surface / <100>
(a “45 degree” wafer)

Both <110> directions are the same.



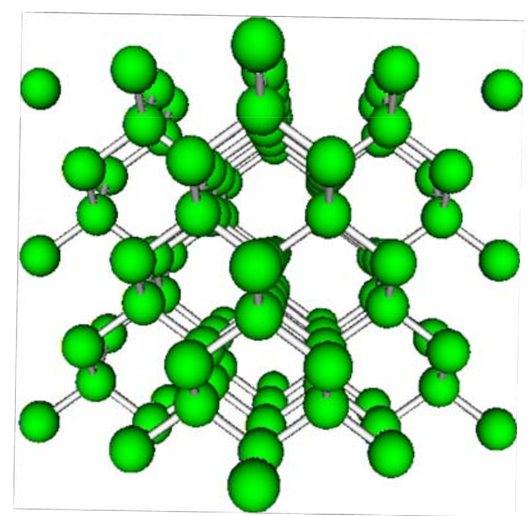
(110) surface – top down



Non-standard

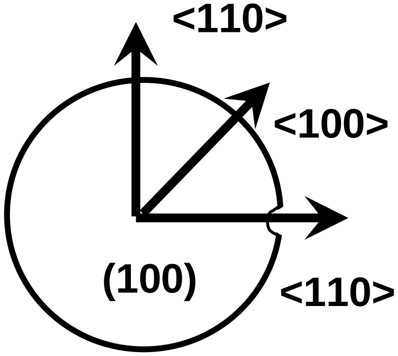
(110) Surface

Three possible channel directions
<110> <111> and <100>



ORIENTATION

(100) surface – top down



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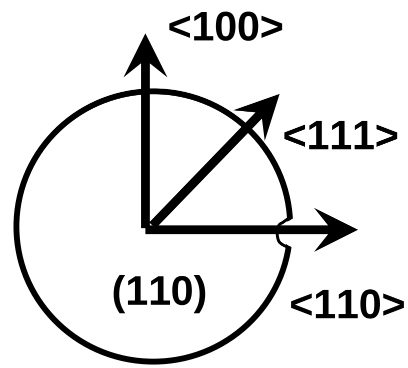
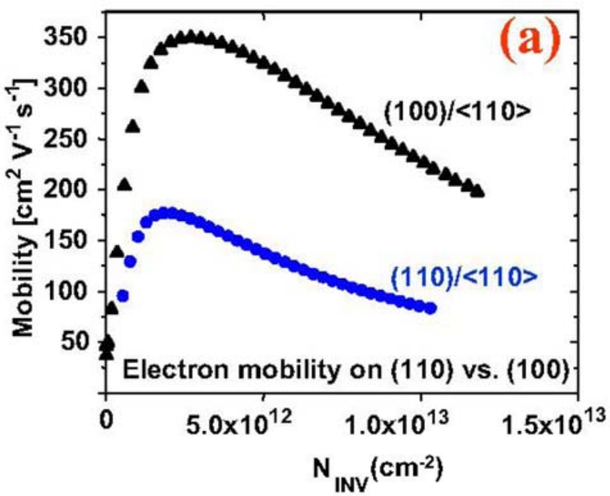


Non-standard

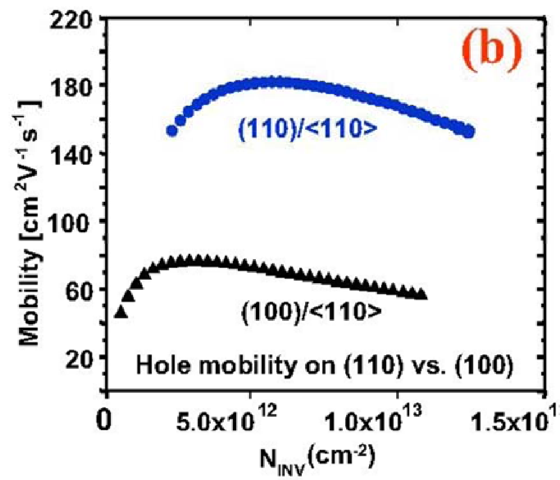
(110) Surface

Three possible channel directions
<110> <111> and <100>

(100) BEST NMOS



(110) <110> BEST PMOS

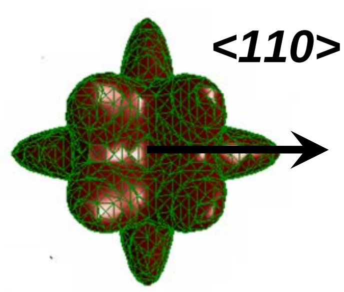


Yang
AMD/IBM
EDST 2007

Orientation and Strain: More complex for non-(100) orientations

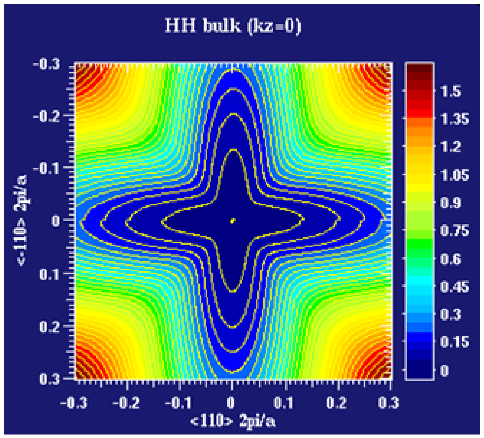
	(001) Surface (k⊥=0)	(001) Surface Vg=-1V	(001) Surface Vg=-1V, Sxx=-1GPa

(100)

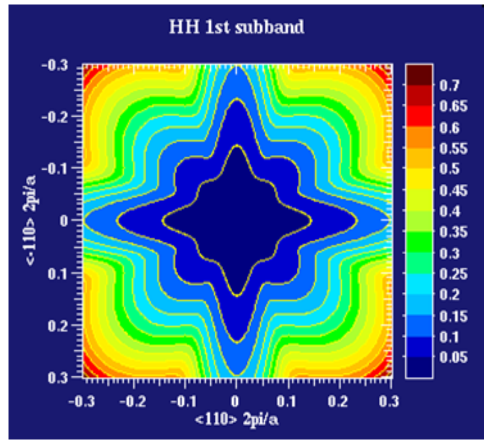


<110>

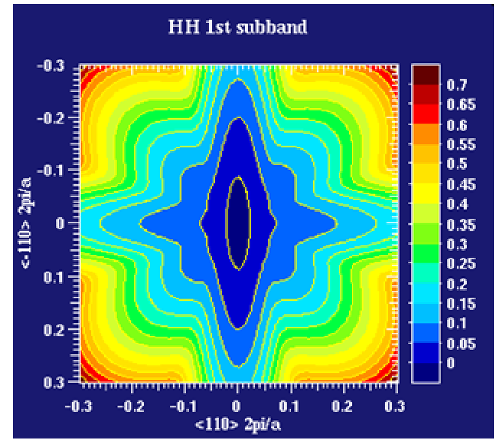
(001) Surface (k⊥=0)



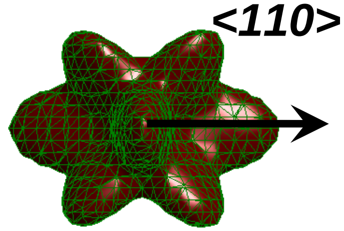
(001) Surface Vg=-1V



(001) Surface
Vg=-1V, Sxx=-1GPa

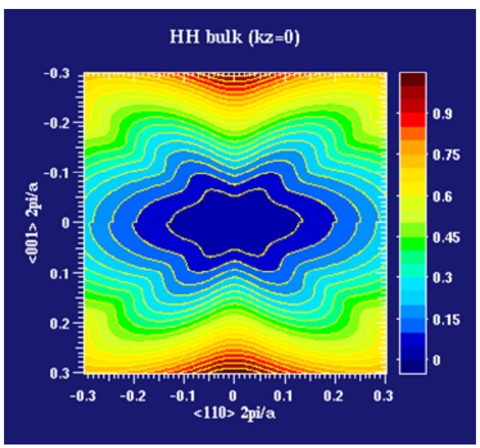


(110)

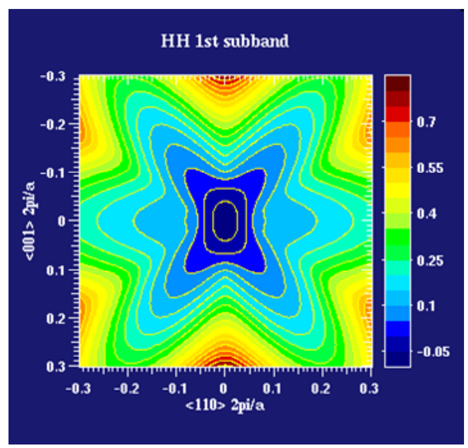


<110>

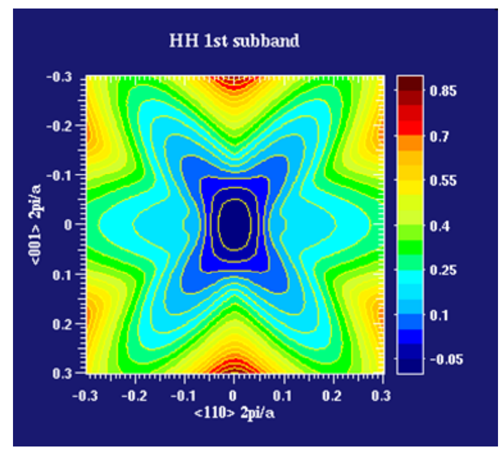
(110) Surface (k⊥=0)



(110) Surface Vg=-1V



(110) Surface
Vg=-1V, Sxx=-1GPa



BULK

1'D CONFINED

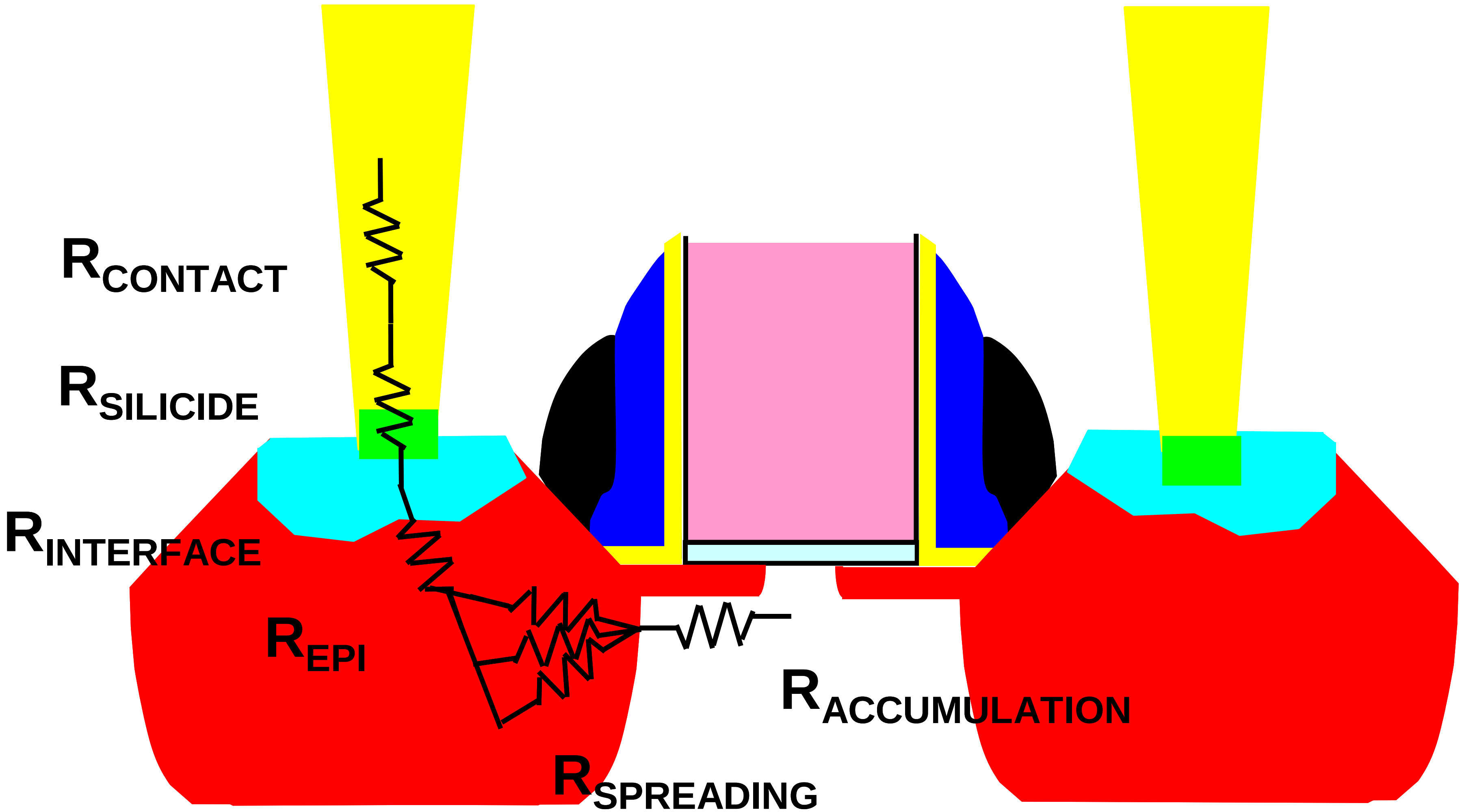
1'D CONFINED STRAINED

Kuhn/Packan, Intel, IEDM 2008

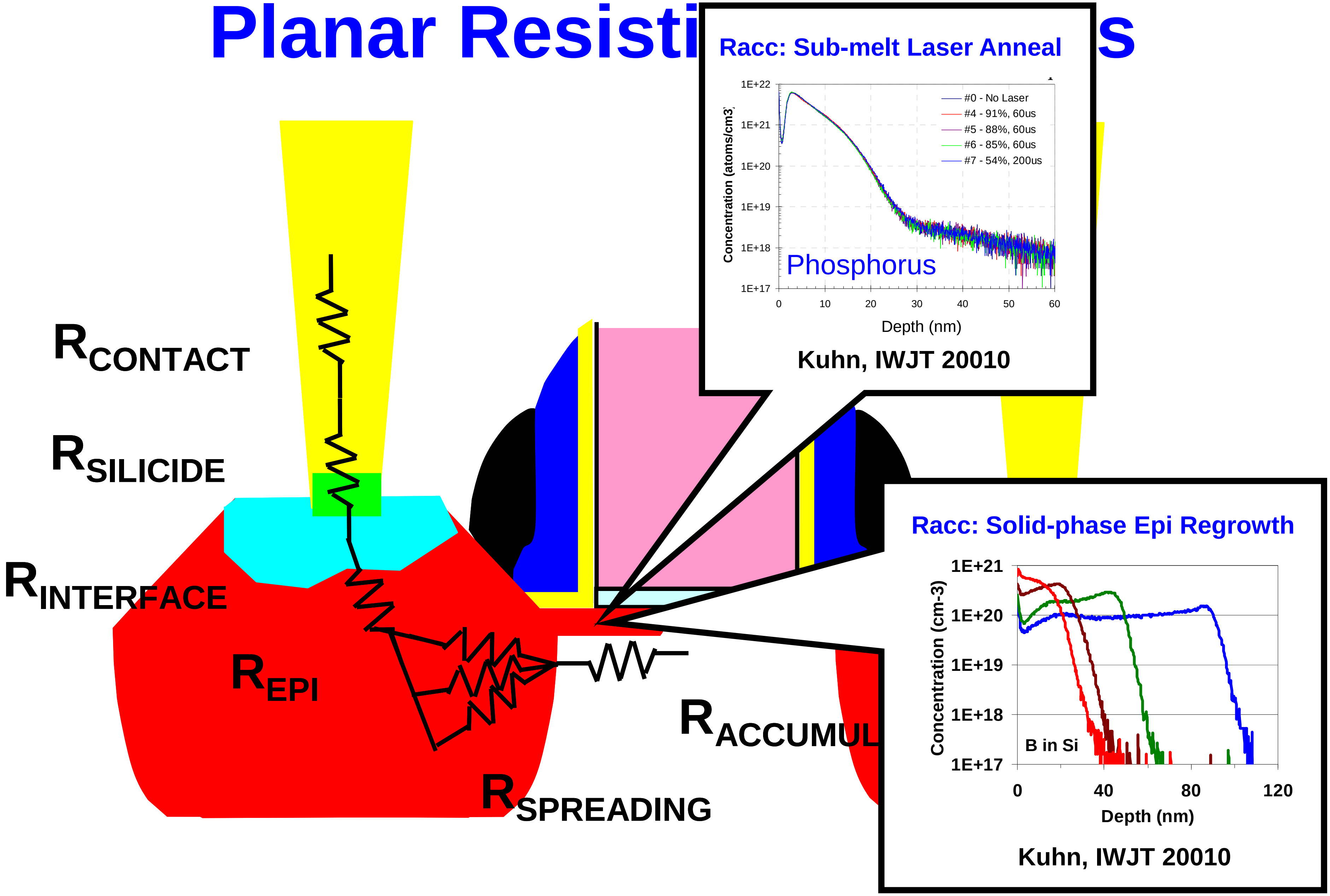
AGENDA

- Scaling
- Gate control
- Mobility
- Resistance
- Capacitance
- Summary

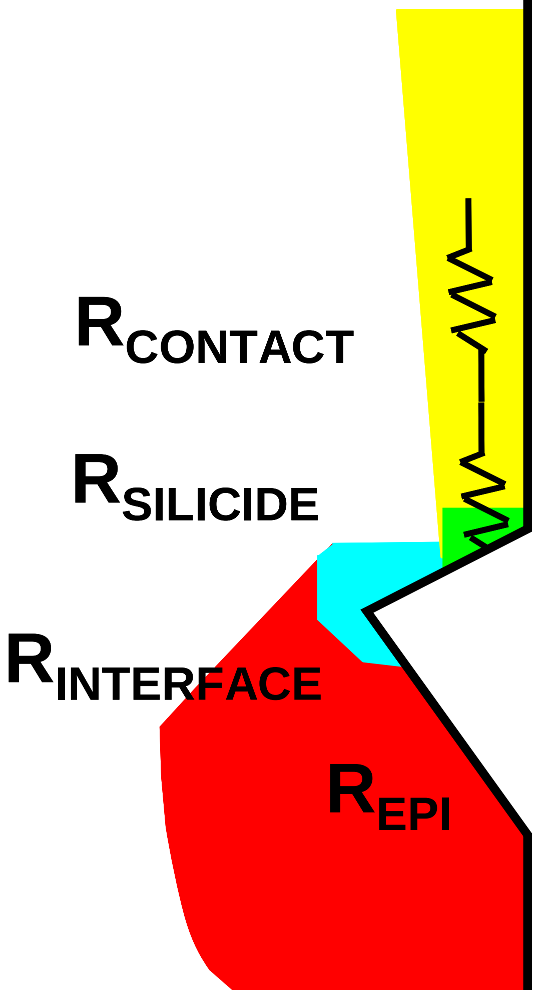
Planar Resistive Elements



Planar Resisti   s

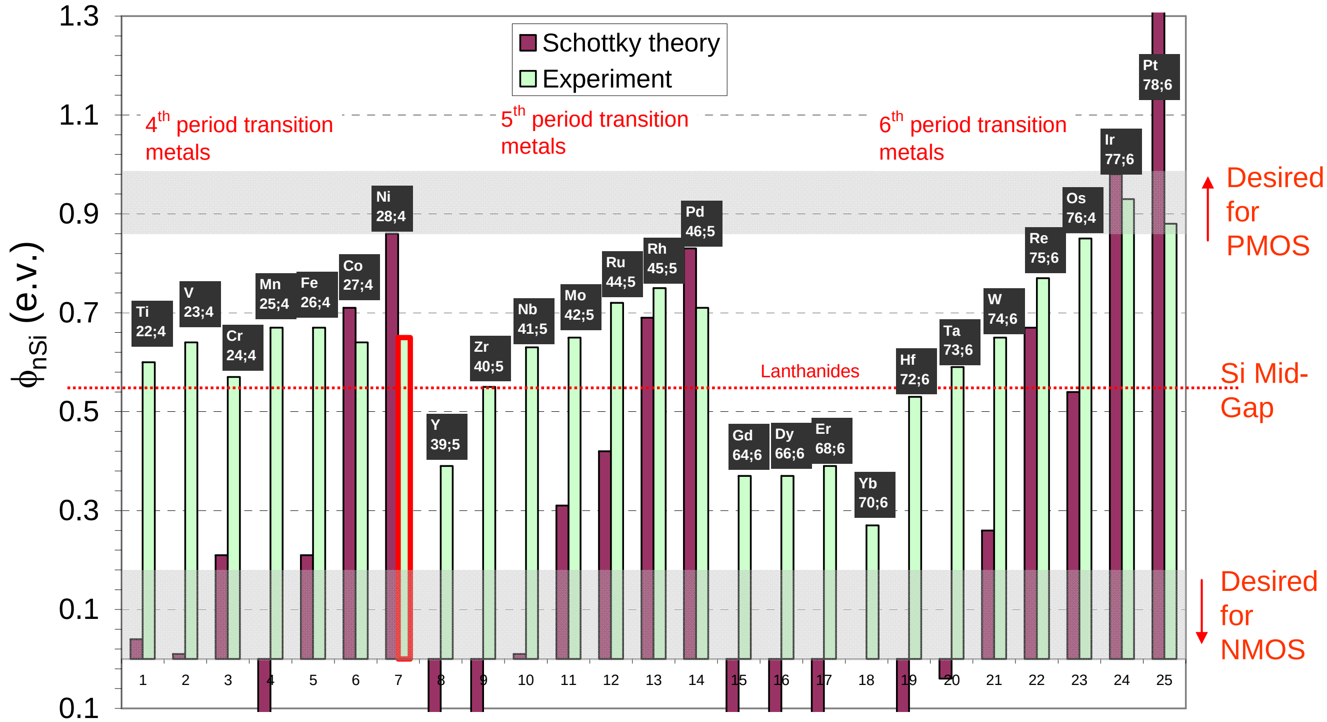


Plan



Rinterface: Reduction in Schottky Barrier Height

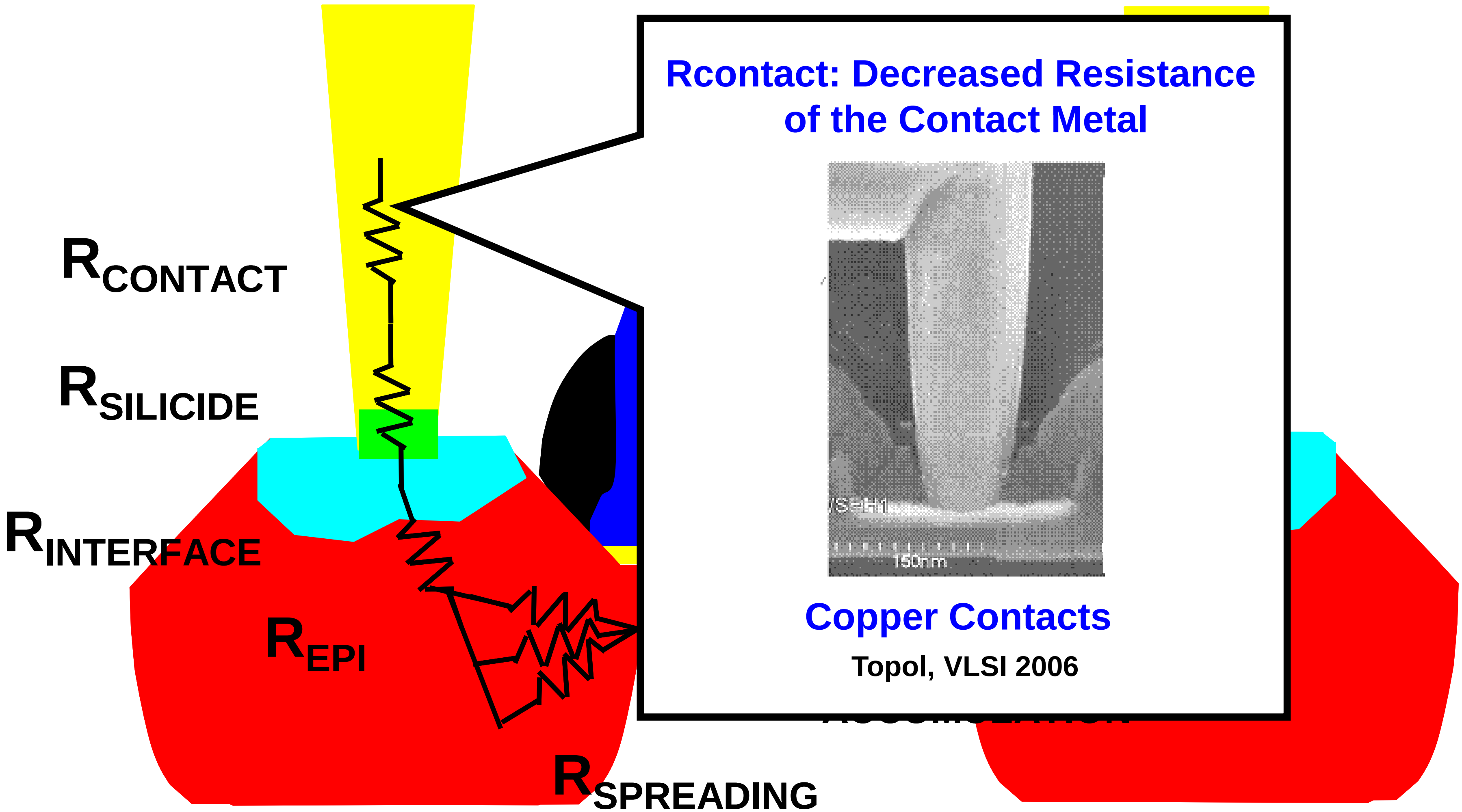
$$R_{\text{interface}} \propto \exp\left(\frac{q\phi_B}{\sqrt{N_D}}\right)$$



Schottky Barrier Height Reduction is a critical area for development. Techniques under investigation include exotic alloys, implants, and Fermi-unpinning layers

Kuhn, IWJT 20010

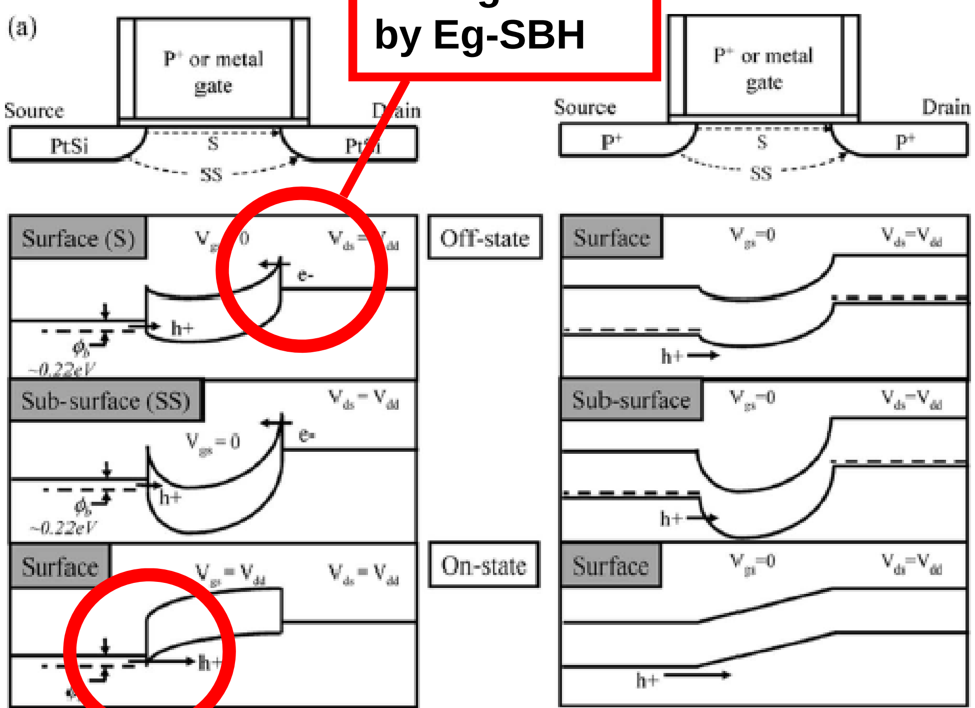
Planar Resistive Elements



Kuhn, IWJT 20010

Schottky barrier S/D – an option?

Electron leakage set by Eg-SBH



Metallic SD ***Conventional***

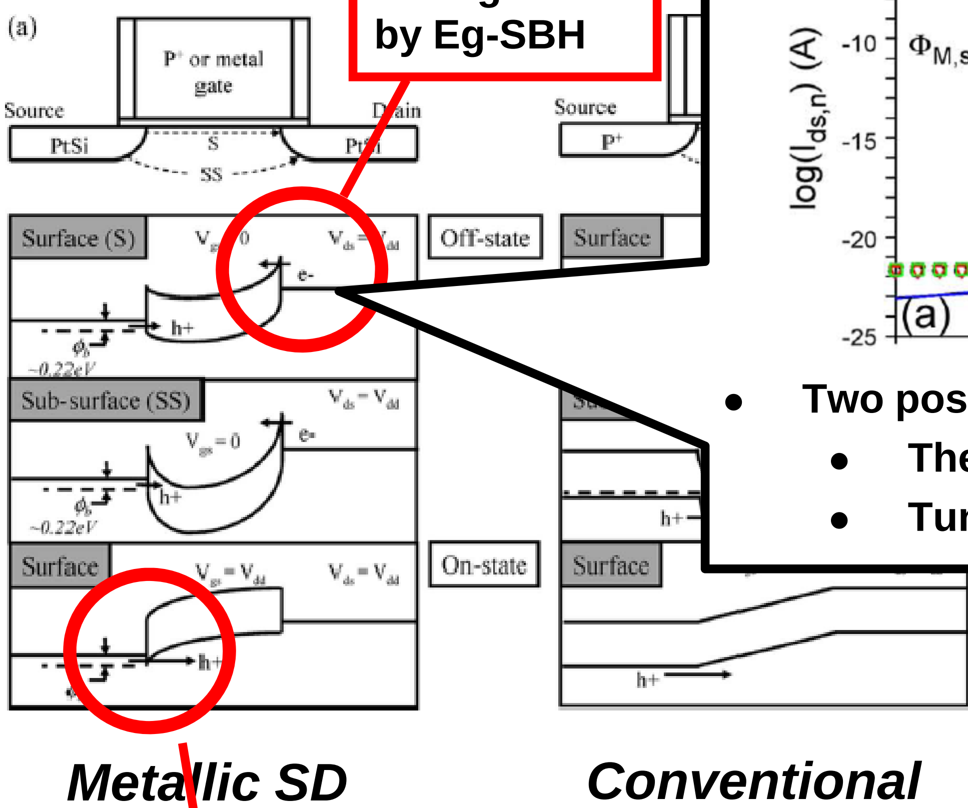
Hole barrier set by SBH

Larson – Spinnaker TED 2006

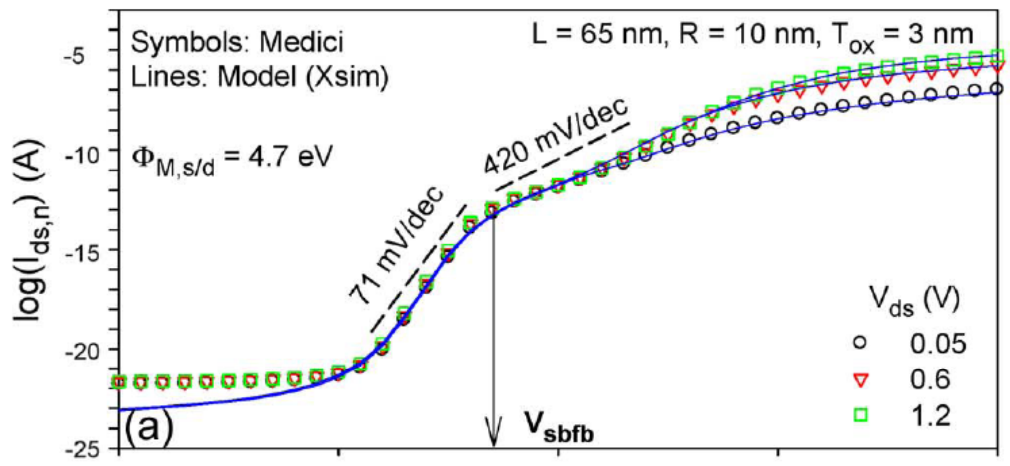
- In a metal SB-MOS, S/D forms an atomically abrupt Schottky-barrier having the height ϕb.
- The extreme limit for metal in the S/D regions (with associated improvements in Rext)
- Unconventional operation (field emission device in the ON state)
- Needs complementary devices (midgap silicide or two silicides)

Schottky barrier S/D – an option?

Electron leakage set by Eg-SBH



Zhu IEEE TED May 2009



- Two possible conduction paths:
  - Thermionic – over the barrier – good SS slope
  - Tunneling – through the barrier – poor SS slope

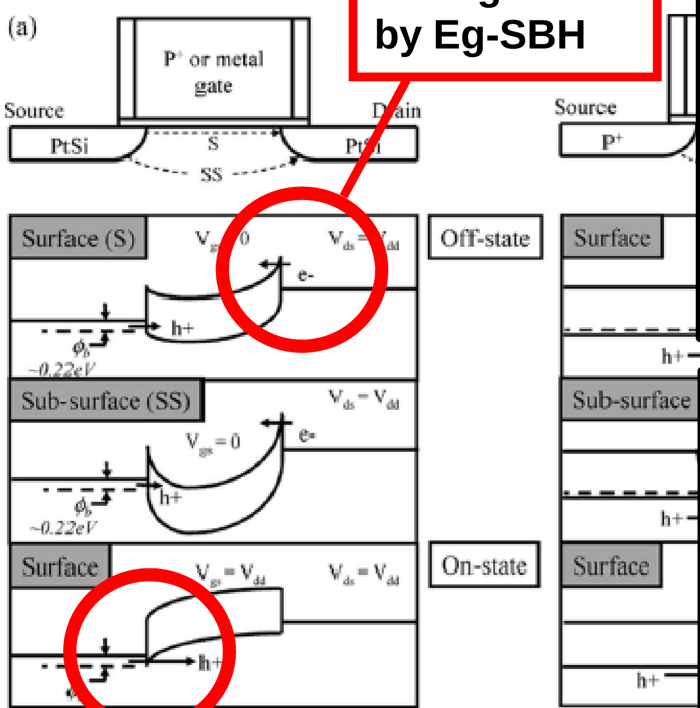
Hole barrier set by SBH

Larson – Spinnaker TED 2006

- Unconventional operation (field emission device in the ON state)
- Needs complementary devices (midgap silicide or two silicides)

Schottky barrier S/D – an option?

Electron leakage set by Eg-SBH



Metallic SD ***Conv***

Hole barrier set by SBH

Larson – Spinnak TED 2006

Benefits

- Low bulk resistance contacts to the channel
- Very abrupt junctions
- No random s/d dopant fluctuation effects
- Minimize s/d carrier-carrier scattering effects

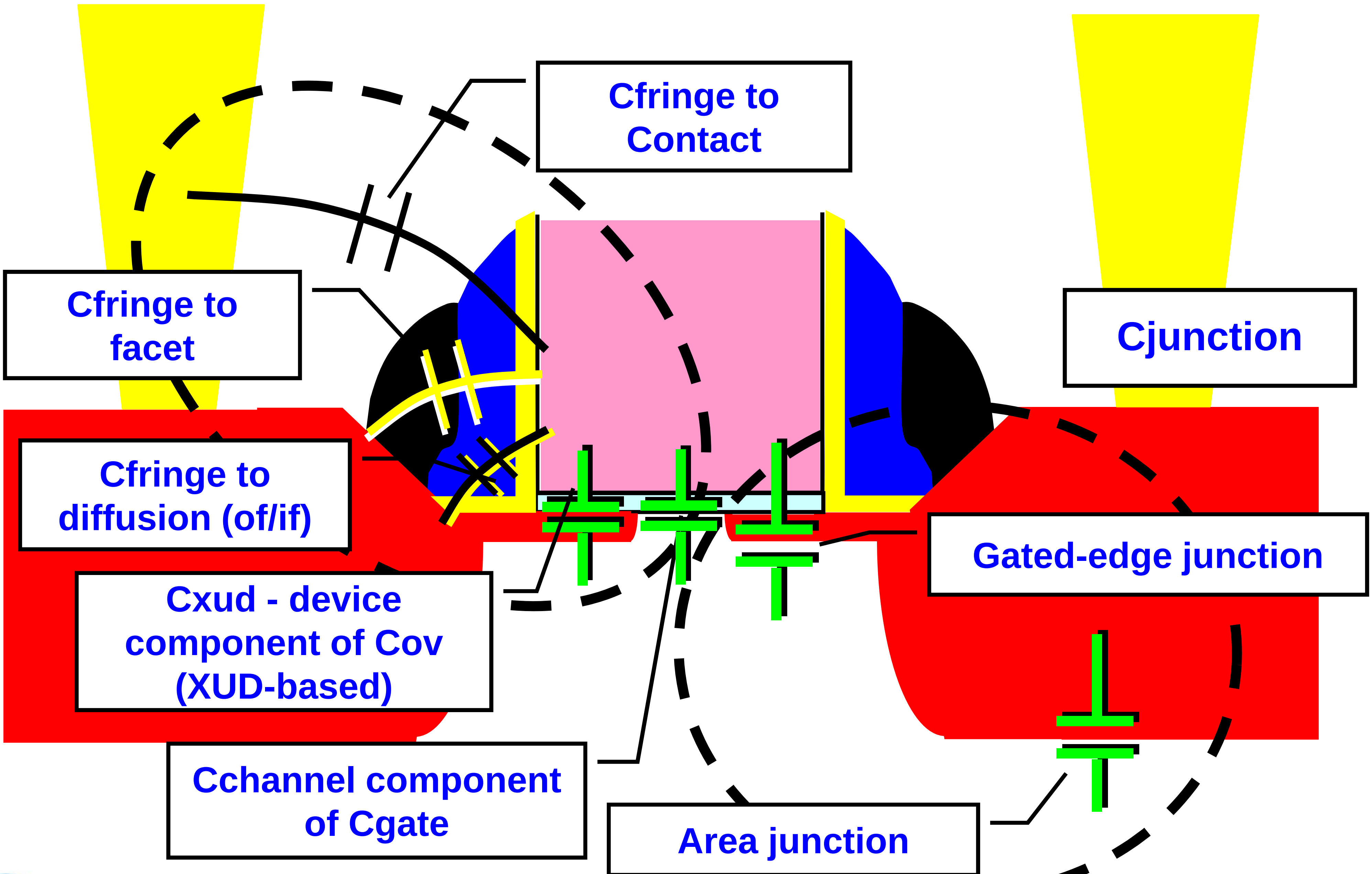
Challenges

- Poor experimental drive currents
- Requires bandedge Schottky barriers
- Ambipolar conduction (high drain-body leakage for bulk devices)
- Early contact formation limits midsection process temperatures
- Need alternative approach for s/d stressors

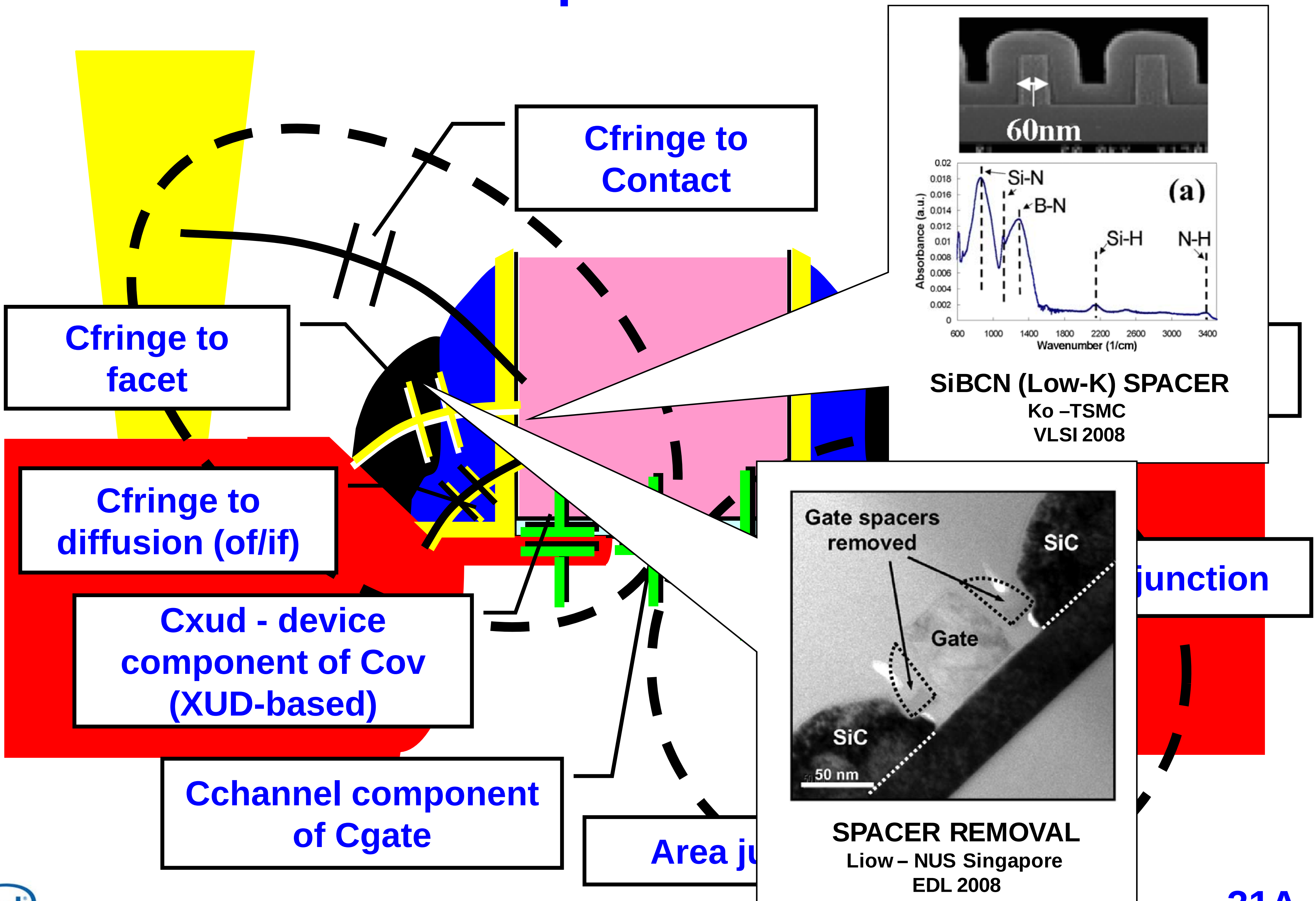
AGENDA

- Scaling
- Gate control
- Mobility
- Resistance
- Capacitance
- Summary

Planar Capacitive Elements



Planar Capacitive Elements



AGENDA

- Scaling
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- Mobility
- Resistance
- Capacitance
- Summary

Looking Forward

Low risk Enhancements in strain technology Enhancements in HiK/MG technology
Medium Risk Optimized substrate and channel orientation Reduction in MOS parasitic resistance Reduction in MOS parasitic capacitance
High risk UTB devices MuGFETS Nanowires 3'D Stacked Devices

Q&A